# BST Capacitors for Cryogenic Focal Plane Arrays

## FINAL REPORT

**Dr. Frank DiMeo**
Principal Investigator

**Contract # DAAL01-97-C-0079**

Sponsored by:
**U.S. Army Research Laboratory**

Contract Period:
**March 10, 1997- June 30, 2000**



ATMI
7 Commerce Drive, Danbury, CT 0681
Phone (203) 794-1100 Fax (203) 792-8040

Executive Summary ..... 2
Introduction ..... 2
Current IRFPA Technology and Limitations ..... 2
High Density Storage Capacitor Technology ..... 4
Project Results ..... 5
Phase II Objectives ..... 5
High Dielectric Materials and Process development ..... 5
Capacitor objectives ..... 6
BST Development ..... 7
Conventional MOCVD Designed Experiment ..... 7
Digital CVD Process Development ..... 19
Amorphous Mixed Oxide Thin Film Development ..... 28
High Pressure, Low Temperature Processing of BST Films ..... 28
Rapid Thermal Annealing Process Experiments ..... 34
Cryogenic Measurements of Amorphous and RTA BST ..... 37
Amorphous mixed oxide dielectric thin films ..... 41
Cryogenic Measurements of Mixed Oxide Films ..... 47
Comparison of BST to mixed oxide films ..... 50
IC Process Integration ..... 52
Summary and Conclusions ..... 55

## Executive Summary

The purpose of this project was to enhance the performance of Infrared Focal Plane Array (IRFPA) detectors through the replacement of $SiO_2$ in the integrating capacitor of each array pixel by a material with a higher dielectric constant. The increase in storage capacity that results from this replacement enables the following: design of more complex circuits in each cell; use of longer integration times with increased sensor standoff range; design of smaller cell sizes for 2-color and un-cooled sensor arrays; and detection of low contrast targets/aim points in the presence of radiation from hot missile domes. In Phase I, the feasibility of realizing a charge storage density increase was demonstrated by depositing high dielectric constant $Ba_{1-x}Sr_xTiO_3$ (BST) thin films using Metal Organic Chemical Vapor Deposition (MOCVD). In phase II, this work was extended, and achieved the following goals: A conventional MOCVD process, developed in Phase I, was optimized for the cryogenic operation of BST thin films. A novel Digital MOCVD process for the fabrication of BST thin films was developed and patented. The use of low deposition temperature amorphous oxide thin films for cryogenic applications was demonstrated. The MOCVD process compatibility with current CMOS chip technology was characterized.

BST films deposited using the conventional process at processing temperatures of 580 °C had storage densities as high as 90 $fF/\mu m^2$ at zero bias voltage, and 77 K. Improved crystallization at lower temperatures via a Digital MOCVD process could provide a route to crystalline BST at temperatures as low as 520°C. Amorphous mixed oxide films deposited at 350 °C had storage densities as high as 13 $fF/\mu m^2$ with a breakdown voltage of 4V at 77K, which represents a significant improvement over current technology at a very attractive thermal budget. BST films grown in the amorphous state and subjected to Rapid Thermal Annealing (RTA) treatments show some improvement over current technology, but is less attractive than the amorphous mixed oxide, having both a lower capacitance density and a higher thermal budget. Neither the 350°C mixed oxide process nor the 580°C continuous BST process cause widespread damage to active device performance in current CMOS technology. These successes have provided multiple processing possibilities for the incorporation of thin film materials with increased storage density in Infrared Focal Plane Arrays (IRFPA).

## Introduction

### *Current IRFPA Technology and Limitations*

Raytheon (formerly: Hughes Santa Barbara Research Center, SBRC) has been a pioneer in extending Infrared Focal Plane Array (IRFPA) technology in size and complexity. They have demonstrated high performance HgCdTe 640 x 480 pixel infrared imaging arrays and 1000 x 1000 pixel InSb infrared imaging arrays as well as detectors with multi-spectral capability. They have also demonstrated 128 x 128 fully integrated 2-color imagers with sequential and simultaneous operation. These accomplishments illustrate the maturity of both HgCdTe and InSb detector technology. However, as the current state of the art has been pushed to accommodate larger arrays, smaller unit cell sizes, and multiple colors per cell, significant limitations have

arisen due to shrinking charge storage per unit cell. Examples of these limitations are given below:

- Limit on Circuit Complexity in the Unit Cell

  Charge transfer per unit cell is an invention pioneered by Hughes in the late 1980s. This concept provides excellent dynamic range, low noise and insensitivity to non-uniformities since charge (not voltage) is extracted. The charge storage requirement of this technique currently limits the size reduction that can be achieved with current generation dielectric materials. Development of materials with increased dielectric constants can be used reduce the cell size, and thus increase cell density.

- Limitations to Effective Use of Integration Time

  Earth looking long wavelength infrared sensors cannot effectively integrate (collect charge) for the full integration time allotted by the parallel to serial readout process. To prevent charge buckets from overflowing, the integration clock time is typically 1/10th of the total readout time. If full integration could be accommodated using higher dielectric constant materials, significant increases in dynamic range could be achieved, with concomitant increases in sensor standoff range for target detection.

- Limit on Cell Sizes for Two-Color Arrays

  A novel multiple bump per unit cell and directional etching techniques have enabled Raytheon to fabricate integrated two color arrays for simultaneous operation. The unit cell size required for the simultaneous design is nearly twice the size of cells for single color IRFPA's due predominately to the additional silicon real estate needed for the second color. A backend high dielectric process would not only decrease the cell size, but could also free up valuable silicon chip real estate.

- Increased Sensitivity of Uncooled IRFPAs

  Longer integration times provided by high dielectric constant films for the uncooled bolometer IRFPA manufactured at Raytheon will enhance sensitivity.

- Hot Dome Problem

  Reduced detection occurs because of present sensor inability to accommodate the full dynamic range of the flux caused by the heating of the missile dome at high velocities. Increases in dynamic range realized by the incorporation of high dielectric materials would improve the accuracy of aim-point determination as the missile approaches the target.

A number of alternative strategies for increasing the storage capacitance using conventional dielectric materials have been investigated. These include: stacked

capacitors; trench capacitors and 3-D stack geometries. These suffer from limitations on the maximum capacitance increase that can realized, e.g. a factor of 2 to 3 for stack and trench capacitors, or from increased design complexity.

The increase in storage capacity per unit cell enabled by high dielectric constant thin films provides solutions to the above IRFPA problems without the limitations of the alternate approaches. Advantages include: (1) more complex circuits in each unit cell, (2) longer integration times with increased sensor standoff range; (3) smaller cell sizes for 2-color and un-cooled sensor arrays, (4) detection of low contrast targets/aim points in the presence of radiation from hot missile domes.

## *High Density Storage Capacitor Technology*

Solutions to the technological issues related to maximizing the stored charge in the minimum area within an integrated circuit have historically been driven by the DRAM (dynamic random access memory) industry. Early generations of DRAMs used planar $SiO_2$ storage capacitors with dielectric thicknesses of several hundred angstroms. As higher storage densities were required, the DRAM industry first improved the quality of the $SiO_2$ layers allowing thinner dielectrics to be reliably used. In recent DRAM generations, after the theoretical limits of $SiO_2$ were reached, trench and stacked structures have been used to reduce the area of the storage capacitor while decreasing it's projected area.[1] Most DRAM manufacturers are expecting the practical limits of this approach to be reached within the next several years and are actively pursuing new materials to achieve the storage densities needed for 1Gb and beyond.[2]

The requirements for cryogenic focal plane array read-out integrated circuits are similar to those for DRAM storage capacitors - maximum capacitance/area is desired with the minimum leakage current across the capacitor electrodes. Some of the more promising materials thin film properties are summarized below in Table 1.

---

1. For reviews of DRAM storage capacitor technology see:
P. Fazan, Integrated Ferroelectrics, Vol 4 (1994), p247.
L. Parker and A. Tasch, IEEE Circuits and Devices, Jan. 1990, p17.

2. Active research programs on high dielectric constant materials for DRAM storage capacitors exist at virtually all DRAM manufacturers including, IBM, Micron Technology, Mitsubishi, NEC, Sharp, Texas Instruments, Samsung and Goldstar.

Table 1. Summary of high dielectric materials properties. The values shown below for dielectric constant (ε) and storage density (C/A) are for room temperature operation at 1.5V with acceptable leakage current density ($<10^{-6}$ A/cm$^2$).

| High ε Material | Deposition Method | ε | Thickness (Å) | C/A (fF/μm$^2$) |
|---|---|---|---|---|
| $SiO_2$ | | | | 1 |
| $SiN_x$ / $SiO_2$ | | | | 2-3 |
| $Ta_2O_5$ [3] | OCVD | 25 | 160 | 14 |
| $SrTiO_3$ [4] | OCVD | 149 | 310 | 43 |
| BST [5] | Sputtered | 420 | 300 | 124 |
| | OCVD | >300 | 300 | >90 |
| PLT [6] | ol-gel | 1400 | 5000 | 25 |
| PLZT [7] | ol-gel | 1474 | 1500 | 87 |

## Project Results

### *Phase II Objectives*

This phase II program addressed the integration and manufacturing issues that are critical to the incorporation of high dielectric film technology in IRFPA applications. To achieve this, the following tasks were identified: (1) Materials and deposition process development (2) Materials/IC process integration and (3) Device Metrology

### *High Dielectric Materials and Process development*

The pursuit of a high dielectric replacement for $SiO_2$ began with the Barium-Strontium-Titanate (BST) materials system, and was expanded to investigate amorphous mixed oxide system. Four experimental pathways were followed in the development of the BST materials system:

---

3. P. Fazan et. al., *IEEE Electron Dev. Lett.*, EDL-13, (1992) p86 .
4. P. Lasaicherre et. al. , *Integrated Ferroelectrics*, **8**, (1995) pp201.
5. Sputtered BST properties are from:
   T. Kuroiwa et al., *VLSI Symposium Proceedings*, June 1995, (to be published).
6. S. Dey et al., *IEEE Transactions on Electron Devices*, **39**, (1992) p1607.
7. R. Jones et. al., *Appl. Phys. Lett.*, **60** ,8, (1992) p1022 .

1) Statistically designed Experimentation for the Optimization of the conventional process.
2) Development of a novel Digital CVD process.
3) Investigation of the low-temperature/high-pressure deposition.
4) Rapid Thermal annealing of amorphous thin films

The investigation of the mixed oxide materials system consisted of two sequential sets of experiments followed by electrical characterization:

1) Investigation of the effect of composition.
2) Investigation of the effect of thickness at the optimum composition.
3) Investigation of cryogenic electrical properties

Detailed discussion of our experimental results in each of the areas listed above will be presented in subsequent sections. These results, however, are best understood when presented in light of the proposed capacitor property and deposition process objectives, which are discussed first in the next section.

## Capacitor objectives

The proposed capacitor property and deposition process objectives are summarized in Table 2 and Table 3. These objectives were chosen to correspond to properties that we believed could be obtained reproducibly, while also representing a dramatic performance improvement over existing materials. The $SiO_2$ dielectric currently used in IRFPA ROICs and has a capacitance per unit area (C/A) of ~1 fF/$\mu m^2$.[8] Our goal of 40 fF/$\mu m^2$ at ±5V operation represents a 40x improvement in storage capacity. Low leakage current ($i_L$) and high breakdown voltage ($V_{bd}$) must be maintained and are reflected in the capacitor property objectives below. This storage density goal was achieved in Ba-Sr-Ti thin films deposited by MOCVD. The best films had storage densities of over 90 fF/$\mu m^2$ at zero bias, and an average of 55 fF/$\mu m^2$ out to ±5 Volts at 78 K. The leakage current goal was achieved in the positive voltage direction at 78 K.

Table 2. BST capacitor properties objectives.

| Property | Goal** |
|---|---|
| $i_L$ | < $10^{-7}$A/$cm^2$ at ±5V , 77K |
| Vbd | > 10V |
| C/A | > 40 fF/$\mu m^2$ |
| resistance degradation | extrapolated failure > 10 yr. @ 5V |

The initial process objectives are summarized in Table 3 below. The deposition temperature has been a very important aspect of this project, and we have relied on the input from Raytheon in

8. Private communication with John Drab at SBRC, Santa Barbara CA.

determining the maximum tolerable processing temperature. The goals we began with were chosen to be consistent with the capacitor properties goal and to minimize stress and diffusion generated defects in the underlying CMOS circuitry. Subsequent testing in this program (see IC Process Integration experiments on page 62) suggests that 580 °C is an acceptable process temperature, and this process goal was achieved. In addition, Raytheon suggested that a lower *in situ* deposition temperature would be very desirable, preferably less than 400 °C. In response to this suggestion, we have developed a new low temperature process using amorphous mixed oxide films. This has a maximum processing temperature of 350 °C, and has produced a storage density capacity as high as 25 $fF/\mu m^2$. This was viewed quite favorably by Raytheon, as it still represents a significant improvement in charge storage over $SiO_2$ at a processing temperature that allows a range of wider device integration strategies. The process throughput goal was exceeded through the development of a new Digital CVD process technique. Although films deposited with this technique have not produced films with storage densities as high as those deposited by the conventional process, we believe that equivalent performance can be achieved with additional process refinement.

Table 3. Deposition process objectives

| Parameter | Goal* |
|---|---|
| Deposition temperature | < 580°C (in situ)<br>< 450°C (ex-situ) |
| Process throughput | 5 wafers/hour * |

*for a 1000Å thick film this requires a deposition rate of 74 Å/min

## BST Development

### Conventional MOCVD Designed Experiment

The first materials development approach we investigated was the optimization of a conventional thermal BST CVD process using statistically designed experimental techniques. Since the number of adjustable processing parameters is quite large, a full factorial experiment was not practical to implement. Therefore, we used a fractional factorial block design that examined the 3 most important factors: Ba/Sr Ratio, Growth Temperature and Film Thickness. An experimental design was constructed and films were deposited in a prototype Varian High-K CVD reactor, which is shown in Figure 1.

A central composite design was picked for the experimental matrix, as shown in the Figure 2. In this type of design, a central point in process space is chosen, and the corners of cube are explored as well as well as points that are extreme but coaxial with the center point. In addition to these points, additional experiments were done in regions within the cube, in order to improve the modeling fit. Table 4 lists the values of the process values used for this design, and Table 5 lists the values of the other parameters that were held constant.

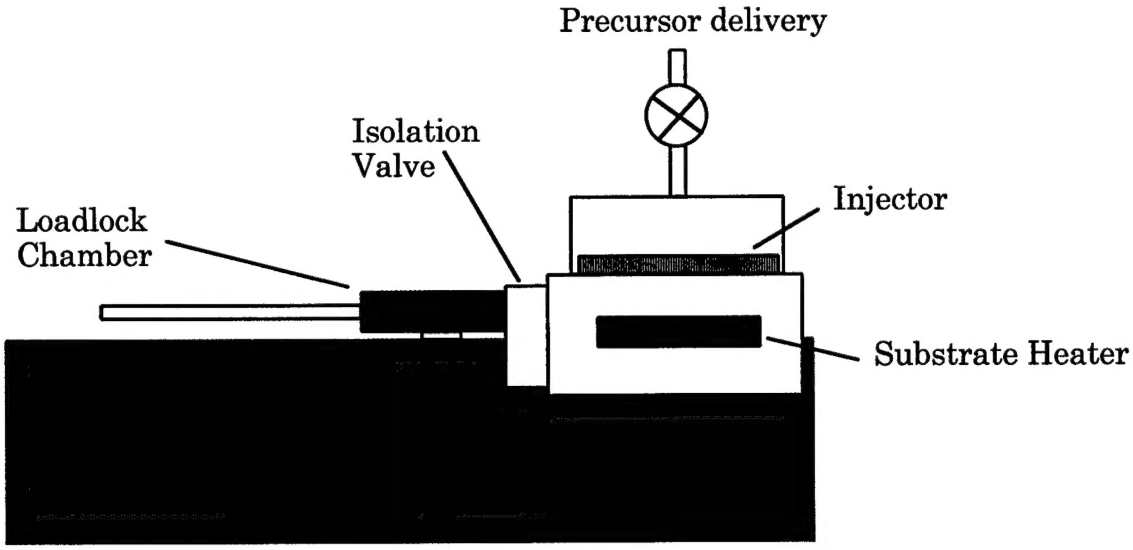



Figure 1. Sketch of the Varian Oxide-CVD reactor, illustrating important features such as the wafer load lock, and the precursor delivery to a showerhead vapor injector for improved uniformity.

Figure 2. Central Composite design

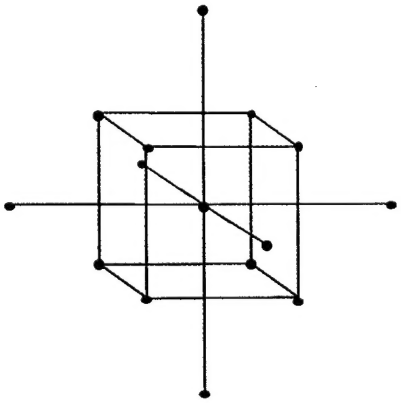


Table 4. Experimental Design Parameters and ranges

| | % Ba in GII | Substrate Temp (°C) | Thickness (Å) |
|---|---|---|---|
| Center | 30 | 580 | 1010 |
| Range | 12 | 20 | 470 |
| | | | |
| 0 | 30 | 580 | 1070 |
| 1 | 18 | 600 | 1480 |
| -1 | 42 | 540 | 540 |
| 1.68 | 50 | 614 | 1800 |
| -1.68 | 10 | 546 | 220 |

Table 5. Parameters held constant in the designed experimental.

| **Conditions** | | **CVD Precursors** |
|---|---|---|
| Ti Content: | 52.1% +/-0.3% | $Ba(thd)_2$ -tetraglyme |
| Growth rate | ~30 Å/min | $Sr(thd)_2$ -tetraglyme |
| Pressure | 700 mTorr | $Ti(OPr\text{-}i)_2$ (thd) |
| Flow rates | Ar- 200;<br>$O_2$, $N_2O$- 500 sccm | |

Table 6 is a listing of the growth parameters and the levels investigated in the first experimental design block. Additional films were also deposited to investigate specific regions of the parameter space in further detail.

Room temperature and cryogenic temperature electrical characterization were performed at Raytheon. Electrical characterization consisted of measuring the AC impedance behavior as a function of voltage. An HP 4275A impedance analyzer was used to measure 3 structures per sample at room temperature and at 78 K. The small signal voltage used was 0.1V, the test frequency was 1MHz, and the bias voltage was varied from –5 to 5 volts in 0.25 V steps.

Tables 7 and 8 list the sample number, growth variables and the zero voltage bias electrical properties for the thin films that were used in the optimization study. (The electrical properties listed are the averages of the storage density in $fF/\mu m^2$; the standard deviation of the storage density also in $fF/\mu m^2$; the relative dielectric constant; and the Q factor along with the standard deviation of the Q factor. The averages and standard deviations were calculated from the measurements of 3-5 structures per sample)

Figures 3 and 4 show a series of plots that are the results of modeling the measurements from Tables 7 and 8 using the equation in the upper right of the figure. The data analysis was done using the software package JMP. These plots are 2-D slices of the 4-D space represented by the three process variables and the given response variable. In this figure, three response variables are displayed, the storage density, the dielectric constant, and the quality factor. The curves in each box are for the conditions fixed by the intersection of the red line in the adjacent plots. For example, the first plot in the upper left, shows the behavior of the storage density vs. the Ba/(Ba+Sr) ratio, with the thickness fixed at 884 Å, and the growth temperature fixed at 580 C.

The first part of an analysis of this type is to determine which of the response variables are important, to what degree are they important, and are there any significant cross effects. To do this we began by looking at the fitting model that included all second order terms as well as first order cross terms. Then, based on the statistical significance of the resulting coefficients, the least probable were removed from the model and the fit was recalculated. This was done iteratively until only coefficients with less than a 0.2 probability of resulting from noise were left. In this way, it was determined that the second order equation shown in the figure was the most appropriate. It should be noted that based on the current data set, no cross terms were found to be significant, however, more experimentation in an area closer to the middle of the process space is needed to further confirm this.

Table 6. Principal Parameters and their levels for the first block of statistical designed experiments. The Ba/Sr ratio was controlled by the appropriate mixing of the liquid precursors. The thickness was determined by the growth time, which had been previously calibrated.

| | DEP RATE | 59 | Å/S | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |
| | | | | | | | | | | |
| | | Ba | Temp | Thick | | | | | | |
| | RANGE | 12 | 20 | 470 | | | | | | |
| | CENTER | 30 | 580 | 1010 | | | | | | |
| | -1 | 18 | 560 | 540 | | | | | | |
| | 1 | 42 | 600 | 1480 | | | | | | |
| | -1.68179 | 10 | 546 | 220 | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| | CC design | | | | | Ba | Substrate | film | Dep | Run |
| | # | Ba | Temp | Thick | | GrII % | Temp. °C | thickness | time | time |
| 1 | 1 | -1 | -1 | -1 | FF | 18 | 560 | 540 | 549 | 24 |
| 2 | 2 | -1 | -1 | 1 | FF | 18 | 560 | 1480 | 1505 | 40 |
| 3 | 3 | -1 | 1 | -1 | FF | 18 | 600 | 540 | 549 | 24 |
| 4 | 4 | -1 | 1 | 1 | FF | 18 | 600 | 1480 | 1505 | 40 |
| 5 | 5 | 1 | -1 | -1 | FF | 42 | 560 | 540 | 549 | 24 |
| 6 | 6 | 1 | -1 | 1 | FF | 42 | 560 | 1480 | 1505 | 40 |
| 7 | 7 | 1 | 1 | -1 | FF | 42 | 600 | 540 | 549 | 24 |
| 8 | 8 | 1 | 1 | 1 | FF | 42 | 600 | 1480 | 1505 | 40 |
| 9 | 9 | -1.68 | 0 | 0 | Axial | 10 | 580 | 1010 | 1027 | 32 |
| 10 | 10 | 1.682 | 0 | 0 | Axial | 50 | 580 | 1010 | 1027 | 32 |
| 11 | 11 | 0 | -1.68 | 0 | Axial | 30 | 546 | 1010 | 1027 | 32 |
| 12 | 12 | 0 | 1.682 | 0 | Axial | 30 | 614 | 1010 | 1027 | 32 |
| 13 | 13 | 0 | 0 | -1.68 | Axial | 30 | 580 | 220 | 223 | 19 |
| 14 | 14 | 0 | 0 | 1.682 | Axial | 30 | 580 | 1800 | 1831 | 46 |
| 15 | 15 | 0 | 0 | 0 | Center -Ax | 30 | 580 | 1010 | 1027 | 32 |
| 16 | 15 | 0 | 0 | 0 | Center -Ax | 30 | 580 | 1010 | 1027 | 32 |
| 17 | 15 | 0 | 0 | 0 | Center -Ax | 30 | 580 | 1010 | 1027 | 32 |
| 18 | 15 | 0 | 0 | 0 | Center -Ax | 30 | 580 | 1010 | 1027 | 32 |
| 19 | 15 | 0 | 0 | 0 | Center -Ax | 30 | 580 | 1010 | 1027 | 32 |
| 20 | 15 | 0 | 0 | 0 | Center -Ax | 30 | 580 | 1010 | 1027 | 32 |

Table 7. Electrical Characterization of BST sample set at 298 K, 0V bias

| Sample | Substrate | Thicknes | At% Ba | At% Sr | At% Ti | Ba/(Ba+Sr | Electrode | C/A | SD C/A | K | Q | SD Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VA1817 | 582.5 | 872.9 | 23.645 | 23.216 | 53.139 | 50.45774 | TI | 38.28489 | 1.198324 | 377.4439 | 9.419041 | 0.74779 . |
| VA1825 | 564 | 481.7 | 21.403 | 26.675 | 51.923 | 44.51724 | TI | 51.65965 | 5.363936 | 281.0533 | 9.313857 | 0.320609 . |
| VA1826 | 564 | 1289.8 | 20.191 | 27.322 | 52.487 | 42.49574 | TI | 30.00355 | 1.325472 | 437.0745 | 10.34161 | 2.389838 . |
| VA1829 | 601 | 482 | 20.789 | 27.049 | 52.162 | 43.45708 | TI | 42.78096 | 0.106895 | 232.8939 | 22.46903 | 6.641541 . |
| VA1830 | 601 | 1271.6 | 19.95 | 27.602 | 52.449 | 41.95407 | TI | 28.47098 | 0.699934 | 408.8965 | 18.59672 | 3.228102 . |
| VA1835 | 615.8 | 269.8 | 21.807 | 26.569 | 51.624 | 45.07814 | ATMI | 79.91713 | 4.092036 | 243.5243 | 19.71559 | 0.726444 . |
| VA1837 | 545.5 | 895.5 | 14.997 | 33.057 | 51.946 | 31.20864 | ATMI | 14.16483 | 0.562359 | 143.2641 | 65.48318 | 5.035045 . |
| VA1837 | 545.5 | 895.5 | 14.997 | 33.057 | 51.946 | 31.20864 | TI | 16.55401 | 1.653223 | 167.4285 | 22.64027 | 2.80291 . |
| VA1838 | 615.8 | 889.6 | 14.608 | 33.106 | 52.286 | 30.61575 | ATMI | 80.27532 | 39.77266 | 806.5612 | 21.16677 | 14.39554 . |
| VA1838 | 615.8 | 889.6 | 14.608 | 33.106 | 52.286 | 30.61575 | TI | 67.72472 | 0.44354 | 680.4598 | 24.21047 | 0.463897 . |
| VA1839 | 582.5 | 204.3 | 17.447 | 31.612 | 50.942 | 35.5633 | ATMI | 64.89779 | 48.52883 | 149.7472 | 10.76187 | 7.379034 . |
| VA1839 | 582.5 | 204.3 | 17.447 | 31.612 | 50.942 | 35.5633 | TI | 32.88816 . | | 75.88718 | 0.168671 . | . |
| VA1840 | 582.5 | 889.7 | 14.825 | 33.027 | 52.148 | 30.98094 | ATMI | 34.1151 | 0.332243 | 342.8078 | 30.19463 | 0.283845 . |
| VA1840 | 582.5 | 889.7 | 14.825 | 33.027 | 52.148 | 30.98094 | TI | 73.26575 | 3.087856 | 736.2157 | 19.08434 | 1.703027 . |
| VA1841 | 582.5 | 1574 | 14.464 | 33.352 | 52.185 | 30.24929 | ATMI | 20.27993 | 0.324939 | 360.5218 | 56.85191 | 3.070227 . |
| VA1841 | 582.5 | 1574 | 14.464 | 33.352 | 52.185 | 30.24929 | TI | 19.2176 | 0.340735 | 341.6365 | 22.08112 | 6.441814 . |
| VA1851 | 564 | 476.6 | 9.86 | 38.44 | 51.57 | 20.41408 | ATMI | 32.92081 | 3.141827 | 177.2087 | 42.35191 | 2.294414 . |
| VA1851 | 564 | 476.6 | 9.86 | 38.44 | 51.57 | 20.41408 | TI | 38.1207 | 5.304838 | 205.1991 | 10.99408 | 0.966289 . |
| VA1852 | 564 | 1274.5 | 8.877 | 39.179 | 51.944 | 18.4722 | ATMI | 18.55525 | 0.135444 | 267.0958 | 72.28727 | 8.84888 . |
| VA1852 | 564 | 1274.5 | 8.877 | 39.179 | 51.944 | 18.4722 | TI | 18.36078 | 1.492508 | 264.2965 | 21.79069 | 0.992514 . |
| VA1853 | 564 | 884.8 | 8.988 | 38.934 | 52.079 | 18.75548 | ATMI | 26.03591 | 0.023923 | 260.1827 | 54.48119 | 3.547574 . |
| VA1855 | 564 | 872.6 | 9.044 | 38.78 | 52.177 | 18.91101 | ATMI | 20.39319 | 2.800293 | 200.9837 | 64.12616 | 2.00607 . |
| VA1856 | 564 | 868.9 | 9.038 | 38.749 | 52.213 | 18.91309 | ATMI | 24.50276 | 1.696193 | 240.4614 | 55.6805 | 6.104805 . |
| VA1859 | 564 | 1549 | 8.611 | 39.076 | 52.264 | 18.05733 | ATMI | 11.19153 | 1.087659 | 195.7949 | 83.0108 | 28.87773 . |
| VA1860 | 601 | 467.6 | 9.69 | 38.195 | 52.115 | 20.23598 | ATMI | 39.28913 | 0.299024 | 207.4949 | 39.37767 | 3.713122 . |
| VA1860 | 601 | 467.6 | 9.69 | 38.195 | 52.115 | 20.23598 | TI | 41.59269 | 3.193587 | 219.6605 | 10.08582 | 0.926562 . |
| VA1861 | 601 | 1257.7 | 8.738 | 39.05933 | 52.20367 | 18.28142 | ATMI | 16.89595 | 0.690521 | 240.0049 | 70.23316 | 13.31997 . |
| VA1861 | 601 | 1257.7 | 8.738 | 39.05933 | 52.20367 | 18.28142 | TI | 19.92234 | 0.26457 | 282.9944 | 61.58197 | 17.13181 . |
| VA1862 | 552.9 | 883 | 9.161 | 38.875 | 51.964 | 19.07111 | ATMI | 22.1768 | 0.331296 | 221.1668 | 59.59973 | 4.59608 . |
| VA1863 | 582.5 | 874 | 9.027 | 38.837 | 52.137 | 18.85969 | ATMI | 24.42265 | 0.145205 | 241.082 | 58.69143 | 4.498714 . |
| VA1864 | 582.5 | 1534.2 | 8.743 | 39.118 | 52.139 | 18.26748 | ATMI | 14.98711 | 0.081496 | 259.693 | 72.5556 | 1.920625 . |
| VA1865 | 582.5 | 477.8 | 9.723 | 38.262 | 52.015 | 20.26258 | ATMI | 35.14549 | 0.760418 | 189.6602 | 39.57686 | 2.206016 . |
| VA1867 | 582.5 | 886.1 | 5.453 | 42.425 | 52.123 | 11.38936 | ATMI | 20.32965 | 0.209551 | 203.4572 | 74.7699 | 4.91383 . |
| VA1868 | 564 | 484.4 | 6.11 | 42 | 51.89 | 12.70006 | ATMI | 34.81031 | 1.094266 | 190.4463 | 47.76828 | 3.72411 . |
| VA1869 | 564 | 891.8 | 5.424 | 42.501 | 52.076 | 11.31768 | ATMI | 19.75046 | 0.390885 | 198.9322 | 57.24637 | 5.24626 . |
| VA1871 | 601 | 882.5 | 5.391 | 42.42 | 52.189 | 11.27565 | ATMI | 21.67219 | 0.575981 | 216.0121 | 68.83304 | 1.576192 . |
| VA1872 | 552.9 | 888.2 | 5.504 | 42.503 | 51.993 | 11.46499 | ATMI | 18.6372 | 4.70817 | 186.9614 | 49.7009 | 3.646248 . |
| VA1873 | 582.5 | 877.3 | 5.424 | 42.379 | 52.198 | 11.34657 | ATMI | 22.69613 | 0.603096 | 224.885 | 65.30196 | 5.5847 . |
| VA1873 | 582.5 | 877.3 | 5.424 | 42.379 | 52.198 | 11.34657 | TI | 38.81409 | 1.711207 | 384.5901 | 83.90765 | 5.451512 . |

Table 8. Electrical Characterization of BST sample set at 78 K, 0V bias

| Sample | Thicknes | Substrate | At% Ba | At % Sr | At % Ti | Ba/(Ba+Sr | Electrode | C/A | SD C/A | K | Q | SD Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VA1817 | 582.5 | 872.9 | 23.645 | 23.216 | 53.139 | 50.45774 | TI | 39.72763 | 1.165172 | 391.6676 | 29.39591 | 17.66541 . |
| VA1825 | 564 | 481.7 | 21.403 | 26.675 | 51.923 | 44.51724 | TI | 60.62477 | 6.459774 | 329.8278 | 26.52325 | 5.774647 . |
| VA1826 | 564 | 1289.8 | 20.191 | 27.322 | 52.487 | 42.49574 | TI | 35.47405 | 1.377237 | 516.7656 | 34.43198 | 1.310944 . |
| VA1829 | 601 | 482 | 20.789 | 27.049 | 52.162 | 43.45708 | TI | 45.6784 | 0.180001 | 248.6671 | 37.36627 | 15.23616 . |
| VA1830 | 601 | 1271.6 | 19.95 | 27.602 | 52.449 | 41.95407 | TI | 38.58074 | 0.968552 | 554.0915 | 22.69289 | 5.363892 . |
| VA1835 | 615.8 | 269.8 | 21.807 | 26.569 | 51.624 | 45.07814 | ATMI | 40.79742 | 0.523095 | 124.3183 | 0.968401 | 0.032661 . |
| VA1837 | 545.5 | 895.5 | 14.997 | 33.057 | 51.946 | 31.20864 | ATMI | 20.06814 | 3.730678 | 202.9706 | 40.15749 | 2.849095 . |
| VA1837 | 545.5 | 895.5 | 14.997 | 33.057 | 51.946 | 31.20864 | TI | 21.27118 | 2.166284 | 215.1383 | 43.02092 | 13.32775 . |
| VA1838 | 615.8 | 889.6 | 14.608 | 33.106 | 52.286 | 30.61575 | ATMI | 82.51381 | 19.1083 | 829.0523 | 13.06741 | 1.466815 . |
| VA1838 | 615.8 | 889.6 | 14.608 | 33.106 | 52.286 | 30.61575 | TI | 105.2609 | 2.741997 | 1057.602 | 34.36969 | 0.101992 . |
| VA1839 | 582.5 | 204.3 | 17.447 | 31.612 | 50.942 | 35.5633 | ATMI | 111.0866 | 18.26534 | 256.3246 | 16.72077 | 24.897 . |
| VA1839 | 582.5 | 204.3 | 17.447 | 31.612 | 50.942 | 35.5633 | TI | 120.3012 . | | 277.5867 | 19.69642 . | . |
| VA1840 | 582.5 | 889.7 | 14.825 | 33.027 | 52.148 | 30.98094 | ATMI | 91.87845 | 14.14292 | 923.2467 | 22.80746 | 13.8967 . |
| VA1840 | 582.5 | 889.7 | 14.825 | 33.027 | 52.148 | 30.98094 | TI | 107.3223 | 1.854719 | 1078.435 | 33.49556 | 0.683754 . |
| VA1841 | 582.5 | 1574 | 14.464 | 33.352 | 52.185 | 30.24929 | ATMI | 76.39963 | 1.481532 | 1358.177 | 32.05378 | 0.675652 . |
| VA1841 | 582.5 | 1574 | 14.464 | 33.352 | 52.185 | 30.24929 | TI | 37.05616 | 1.098481 | 658.7577 | 20.5885 | 12.06692 . |
| VA1851 | 564 | 476.6 | 9.86 | 38.44 | 51.57 | 20.41408 | ATMI | 97.01657 | 12.45526 | 522.2284 | 19.07887 | 2.289786 . |
| VA1851 | 564 | 476.6 | 9.86 | 38.44 | 51.57 | 20.41408 | TI | 55.32208 | 8.803661 | 297.792 | 31.02318 | 4.702026 . |
| VA1852 | 564 | 1274.5 | 8.877 | 39.179 | 51.944 | 18.4722 | ATMI | 36.51473 | 0.379574 | 525.6158 | 72.74937 | 3.655289 . |
| VA1852 | 564 | 1274.5 | 8.877 | 39.179 | 51.944 | 18.4722 | TI | 36.7358 | 2.949516 | 528.7981 | 39.80393 | 1.34942 . |
| VA1853 | 564 | 884.8 | 8.988 | 38.934 | 52.079 | 18.75548 | ATMI | 45.74125 | 0.137161 | 457.1026 | 58.31947 | 15.71965 . |
| VA1855 | 564 | 872.6 | 9.044 | 38.78 | 52.177 | 18.91101 | ATMI | 30.907 | 5.063096 | 304.6018 | 63.30137 | 14.01981 . |
| VA1856 | 564 | 868.9 | 9.038 | 38.749 | 52.213 | 18.91309 | ATMI | 42.20902 | 3.723616 | 414.2243 | 60.75882 | 8.758882 . |
| VA1859 | 564 | 1549 | 8.611 | 39.076 | 52.264 | 18.05733 | ATMI | 20.18324 | 2.10718 | 353.1041 | 48.5275 | 16.93349 . |
| VA1860 | 601 | 467.6 | 9.69 | 38.195 | 52.115 | 20.23598 | ATMI | 56.78637 | 0.762217 | 299.9018 | 56.65236 | 9.850335 . |
| VA1860 | 601 | 467.6 | 9.69 | 38.195 | 52.115 | 20.23598 | TI | 61.71207 | 5.443314 | 325.9156 | 23.89548 | 17.08842 . |
| VA1861 | 601 | 1257.7 | 8.738 | 39.05933 | 52.20367 | 18.28142 | ATMI | 35.79098 | 0.275861 | 508.4065 | 61.4378 | 4.329389 . |
| VA1861 | 601 | 1257.7 | 8.738 | 39.05933 | 52.20367 | 18.28142 | TI | 44.55254 | 0.408793 | 632.8635 | 58.13044 | 0.934592 . |
| VA1862 | 552.9 | 883 | 9.161 | 38.875 | 51.964 | 19.07111 | ATMI | 36.3582 | 0.702952 | 362.5964 | 81.53708 | 5.463631 . |
| VA1863 | 582.5 | 874 | 9.027 | 38.837 | 52.137 | 18.85969 | ATMI | 41.3407 | 3.03968 | 408.0842 | 50.7686 | 41.64755 . |
| VA1864 | 582.5 | 1534.2 | 8.743 | 39.118 | 52.139 | 18.26748 | ATMI | 34.08748 | 0.364822 | 590.6597 | 31.73977 | 19.36752 . |
| VA1865 | 582.5 | 477.8 | 9.723 | 38.262 | 52.015 | 20.26258 | ATMI | 51.71271 | 1.004781 | 279.0641 | 57.03566 | 44.21667 . |
| VA1867 | 582.5 | 886.1 | 5.453 | 42.425 | 52.123 | 11.38936 | ATMI | 37.91068 | 0.442768 | 379.4065 | 85.14317 | 12.27334 . |
| VA1868 | 564 | 484.4 | 6.11 | 42 | 51.89 | 12.70006 | ATMI | 54.72376 | 2.333723 | 299.3922 | 54.8586 | 28.88774 . |
| VA1869 | 564 | 891.8 | 5.424 | 42.501 | 52.076 | 11.31768 | ATMI | 37.06906 | 0.28324 | 373.3701 | 33.16132 | 8.78106 . |
| VA1871 | 601 | 882.5 | 5.391 | 42.42 | 52.189 | 11.27565 | ATMI | 41.27164 | 1.708617 | 411.3646 | 94.26754 | 10.66198 . |
| VA1872 | 552.9 | 888.2 | 5.504 | 42.503 | 51.993 | 11.46499 | ATMI | 30.82873 | 9.264801 | 309.2622 | 81.72048 | 3.273804 . |
| VA1873 | 582.5 | 877.3 | 5.424 | 42.379 | 52.198 | 11.34657 | ATMI | 43.82044 | 0.164568 | 434.1955 | 96.36251 | 5.641054 . |

Given the determination of which equation is statistically best suited to fit the data, it is important to look at the behavior of the results and see if this is consistent with existing physical knowledge of the system. An examination of the room temperature data, Figure 3, indicates that this is the case. For example, the storage density was decreased with increasing film thickness, as it should from the capacitor equation.[9] The dielectric constant, also, increased with increasing film thickness, which is a well-known behavior in this system. In addition, the dielectric constant increased with increasing Ba content. This was expected as the film composition approaches material that has a Curie temperature close to that of room temperature (*70/30 Ba/Sr*).

A different optimal composition was found when we performed a similar analysis of the cryogenic measurement taken at 78 K. In this case, there is a pronounced maximum in the dielectric constant and the storage density as a function of both composition and growth temperature, and Q goes through a maximum as function of thickness. These trends are maintained as the fixed points (red lines) are varied, i.e. as the temperature is changed, the behavior of the Ba and thickness curves is similar. From this analysis, the optimum composition is *30/70 Ba/Sr*, the optimum thickness is 890 Å, and the best growth temperature is 580 °C. A more careful optimization of thickness, which carefully considers the trade-off between breakdown and capacitance density under appropriate test conditions, would be warranted if it is desired to pursue this solution.

Figure 5 is the dielectric response as a function of voltage, at 298 K and at 78 K, for the film grown at these conditions, VA1840. In this figure, the dielectric constant at 78 K and at 0 volts is ~900 and the storage density is ~90 fF/$\mu m^2$. This exceeds the desired target storage density of 40 fF/$\mu m^2$ by more than a factor of two at zero bias. The average storage density out to +/- 5 V is 55 fF/$\mu m^2$, which also exceeds the desired goal. Figure 6 shows the leakage current density for several capacitor structures on the same sample, measured at room temperature. The leakage current is ~$10^{-8}$ A/$cm^2$ from about –2.5 V to ~+3 V.

Figure 7 shows the leakage current at 78 K, measured 6 months from the time of the first measurements, and shows that it possible to maintain low levels of leakage current ($2.3 \times 10^{-7}$ A/$cm^2$ ) out to 5 volts. The asymmetry is most likely due to difference in the top electrode properties and reinforces the need to optimize the entire capacitor structure, including both top and bottom interfaces.

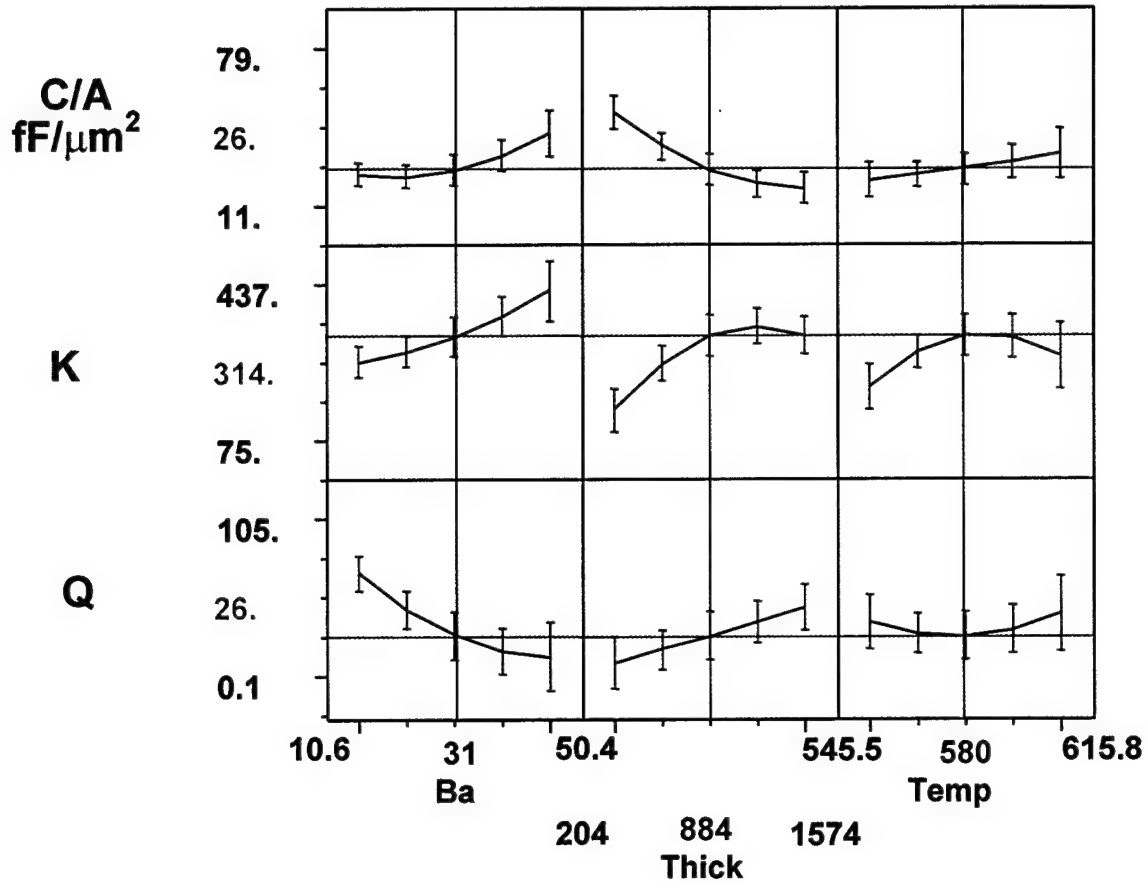
Figure 8 shows the storage density as a function of temperature, taken 6 months from the time of the data in figure 5. The absolute values have decayed somewhat over this time, but the curve remains relatively constant to nearly 200 °K. The decay in absolute value is due to

---

[9] $C/A = \varepsilon\varepsilon_0/T$, where $\varepsilon$ is the relative dielectric constant, and T is the thickness

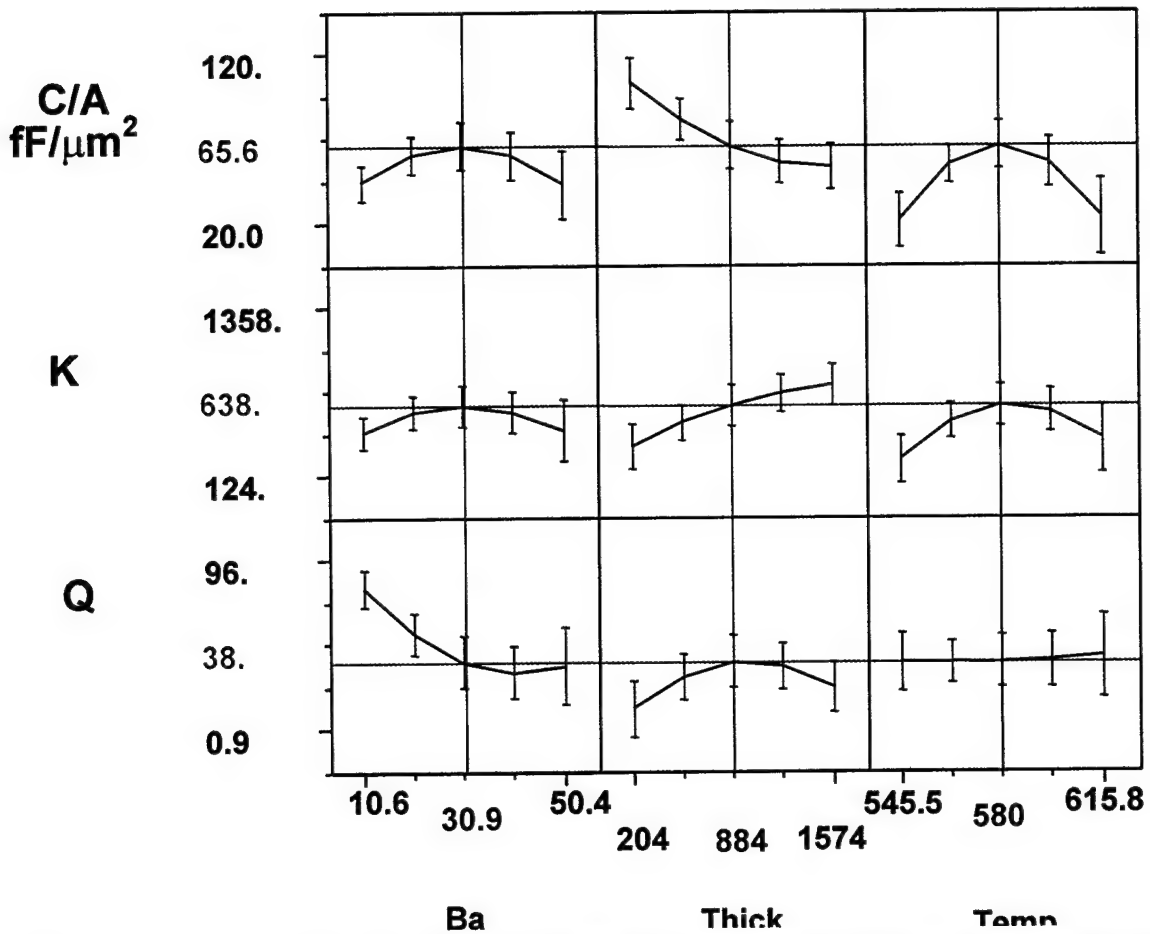
extended air exposure (moisture in particular) and we expect that this can minimized by glass encapsulation, as would be done in a typical integrated device.

In conclusion, the use of a statistically designed experiment resulted in optimizing the growth temperature, composition and thickness of low Ba BST thin films for use at 78 K. We have more than doubled the storage density goal of the project, and have done so with a conventional deposition process, using a temperature that is also within the programs goals. Room temperature leakage current measurements meet the performance goal in the positive bias direction, and with proper top electrode optimization and encapsulation would be expected to perform as well in the negative bias direction.




**Cross terms generally not significant for this data set**

Figure 3. A summary plot of the Screening /Modeling of the result for the statistically design experiment. These are the result of the room temperature electrical characterization




**Cross terms generally not significant for this data set**

Figure 4. A summary plot of the Screening /Modeling of the result for the statistically design experiment. These are the result of the 78 K electrical characterization

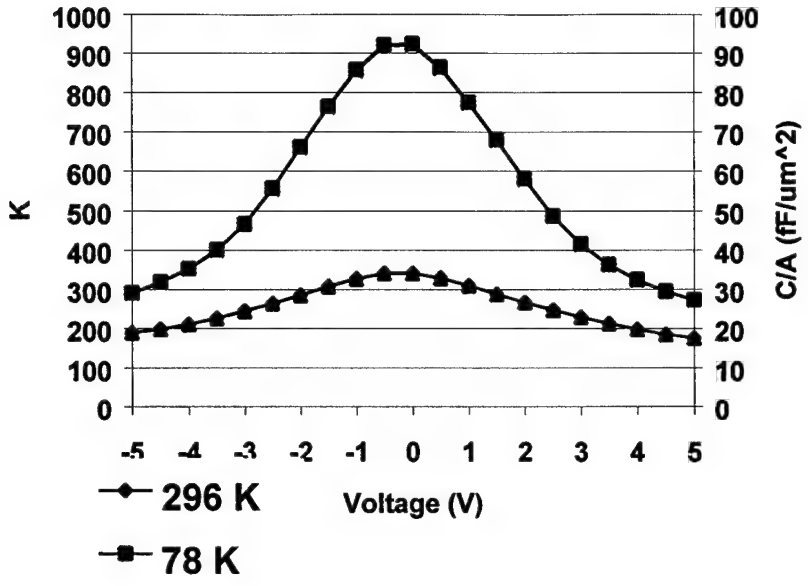



Figure 5. Dielectric Constant and Storage Density as a function of bias voltage at room temperature and 78 K

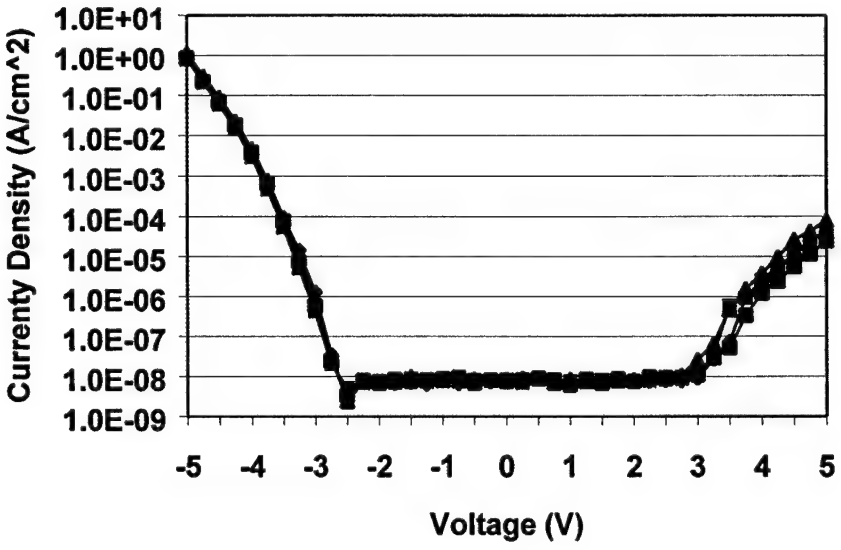



Figure 6. Room temperature leakage current density vs bias voltage for several structures on sample VA1840

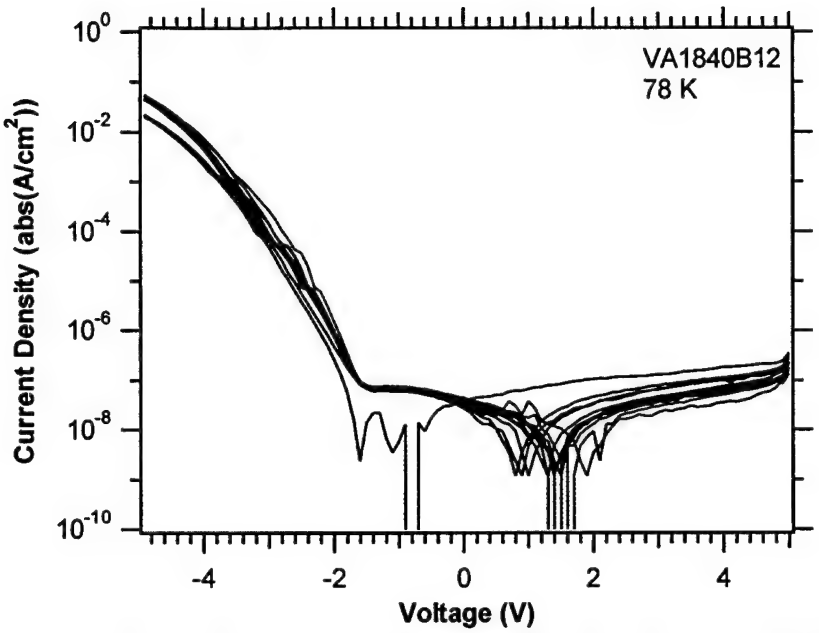



Figure 7 Leakage Current Density vs Voltage for BST thin film VA1840B12 at 78 K

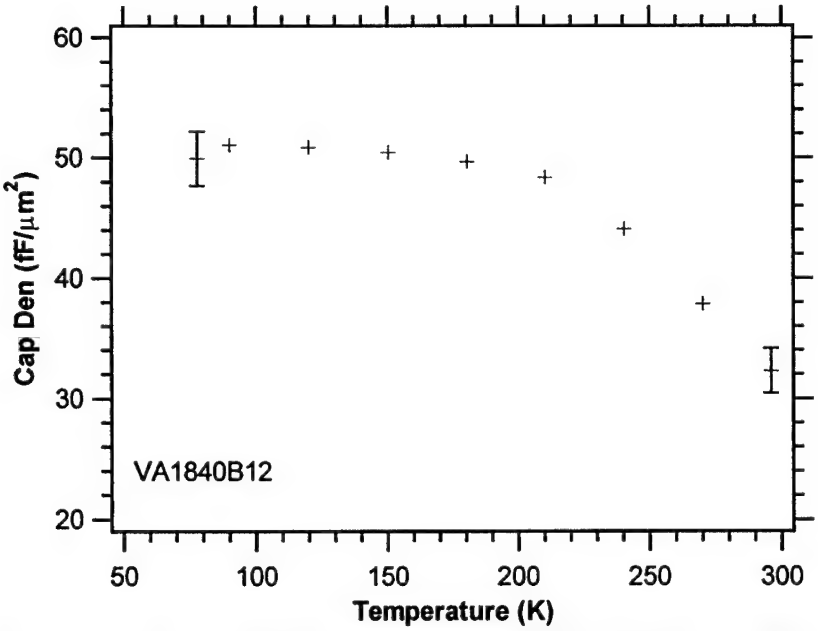



Figure 8 Capacitance Density vs Temperature for BST thin film VA1840B12

## Digital CVD Process Development

The second materials approach investigated was the development of a novel deposition technique known as Digital CVD. This is a technique of temporal separation of the oxidizer species and the precursors. The technique was proposed as a means of inducing crystallinity at a lower temperature by using more aggressive oxidation methods with out detrimental gas phase reaction between the precursors and the oxidizers. There is some precedent for pulsing or separation of precursors in the field of semiconductor CVD, particularly in the fabrication of III-V superlattices and quantum wells. Taken to the ultra high vacuum extreme, this technique becomes known as metal organic molecular beam epitaxy (MOMBE). Our work was the first report of digital CVD as applied to the BST material system, and has been issued as an U.S. patent, US 5,972,430. It is also the only report of digital CVD being used in conjunction with a liquid delivery system. The development of digital CVD resulted in several unexpected improvements over the conventional non—digital growth process in several respects, including increased precursor efficiency, an equalization of efficiency between precursors, lower crystalline deposition temperature, and improved thickness uniformity.

The BST digital CVD experiments were carried out in the Watkin's Johnson CVD reactor, which is similar to the Varian Oxide-CVD reactor illustrated in Figure 1 without the advantage of a load-locked chamber. This reactor is under computer control and a macro program was modified to produce the alternating pulses of precursor, and oxidizer. Figure 9 is schematic of the timing of the pulse trains. The pulses were in the following order: precursor pulse, Ar purge pulse, oxidizer pulse, and purge pulse, and the pulse widths are defined as T1, T2, T3, T4, respectively. Each set of 4 pulses is referred to as one cycle. Table 9 lists typical values for the pulse widths explored to date, as well as other typical growth conditions. The substrates were platinum/tantalum/silicon 5"wafers that were diced into quarters. Typically 2 pieces of wafer were used during each run, and were designated as right and left, (when views facing the front of the reactor)

### Increased Precursor Efficiency

The first improvement we noticed when using the digital mode was a dramatic improvement in the precursor incorporation efficiency. One measure of the aggregate increase of the precursor efficiency is to measure the difference in growth rates. Figure 10 is a plot of growth rate of BST films grown at 560 °C.

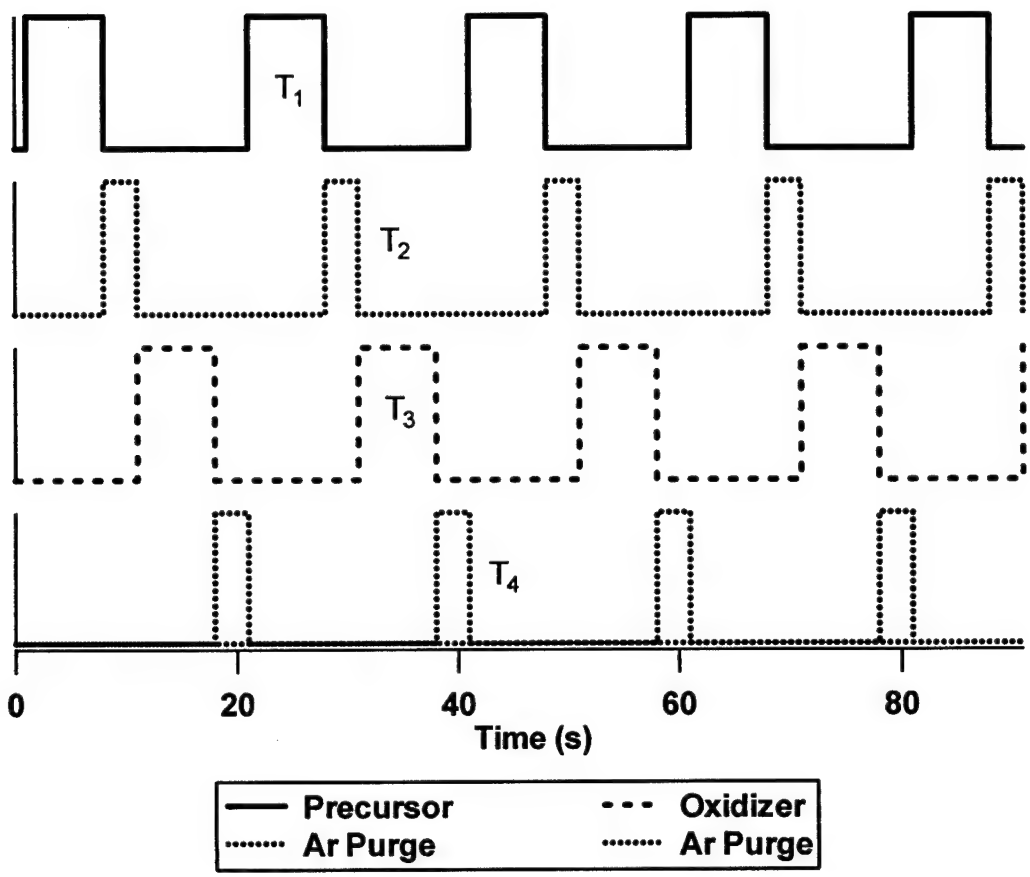



Figure 9. Pulse sequence of precursor, purge and oxidizer gases used in Digital CVD experiments

Table 9. Typical Growth Parameter used to date in Digital CVD processing of BST

| Growth Parameter | Range |
|---|---|
| Precursor Pulse Width, T1 | 7-25 s |
| Ar Purge Pulse Width, T2 | 7-14 s |
| Oxidizer Pulse Width | 7-14 s |
| Ar Purge Pulse Width, T2 | 7-14 s |
| Number of cycles | 50-100 |
| Oxygen flow rate | 500 sccm |
| Nitrous Oxide flow rate | 500 sccm |
| Growth temperature | 420-600 °C |
| Liquid Precursor Flow rate | 0.08 ml/min |
| Growth temperature | 420-600 °C |

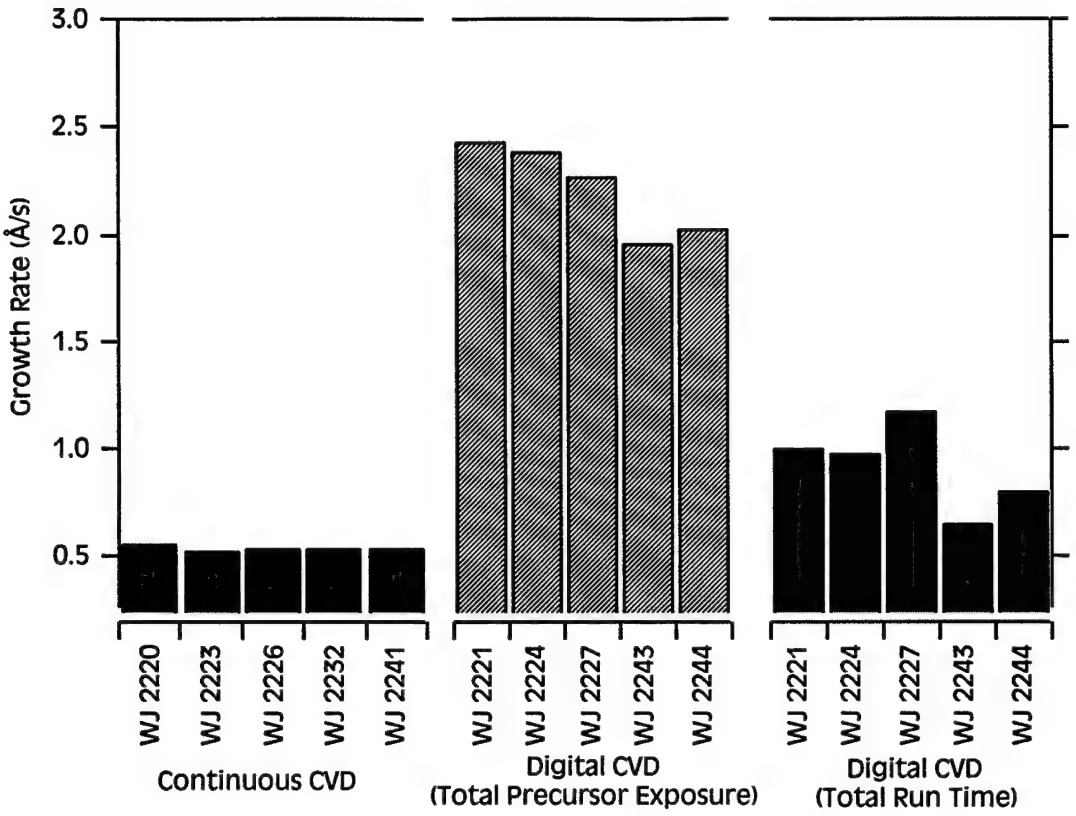



Figure 10. Growth rate vs. sample number for Continuous and Digital CVD processes

The solid gray bars on the left represent the growth rate of films deposited using the continuous CVD process, and are calculated by dividing the thickness measured by XRF by the growth time, which was 1200 s for each of this samples. The broad striped bars in the middle represent the growth rate of films deposited using the Digital CVD process calculated by dividing the thickness by the total precursor exposure time, which was 1400 s for each of these films. The narrow striped bars on the right represent the growth rate of films deposited calculated by dividing the thickness by the total run time, which includes the time of the oxidizer and purge pulses.

The most striking feature of this graph is that there is 4-5 fold increase in growth rate based on precursor exposure. Even after taking into account the oxidizer and purge time, there is better than a factor of 2 improvement in overall growth rate. The use of the digital CVD process provides growth rates that meet the through put goals of 5 wafers/hour. The variability in the digital CVD data occurs because the other pulse widths were being varied during some of these runs to determine how they influenced the growth rate. This is most noticeable by the spread in the total run time data.

Another way to view this data is to look at the individual elemental incorporation efficiencies, as shown in Figure 11. The incorporation efficiencies range from 5-7% in the

continuous process for a relative range of 28 % {(7-5)/7}. The maximum range in the digital process is from 23-27%, which has a much-improved relative range of only 15%, with some samples having even smaller values.

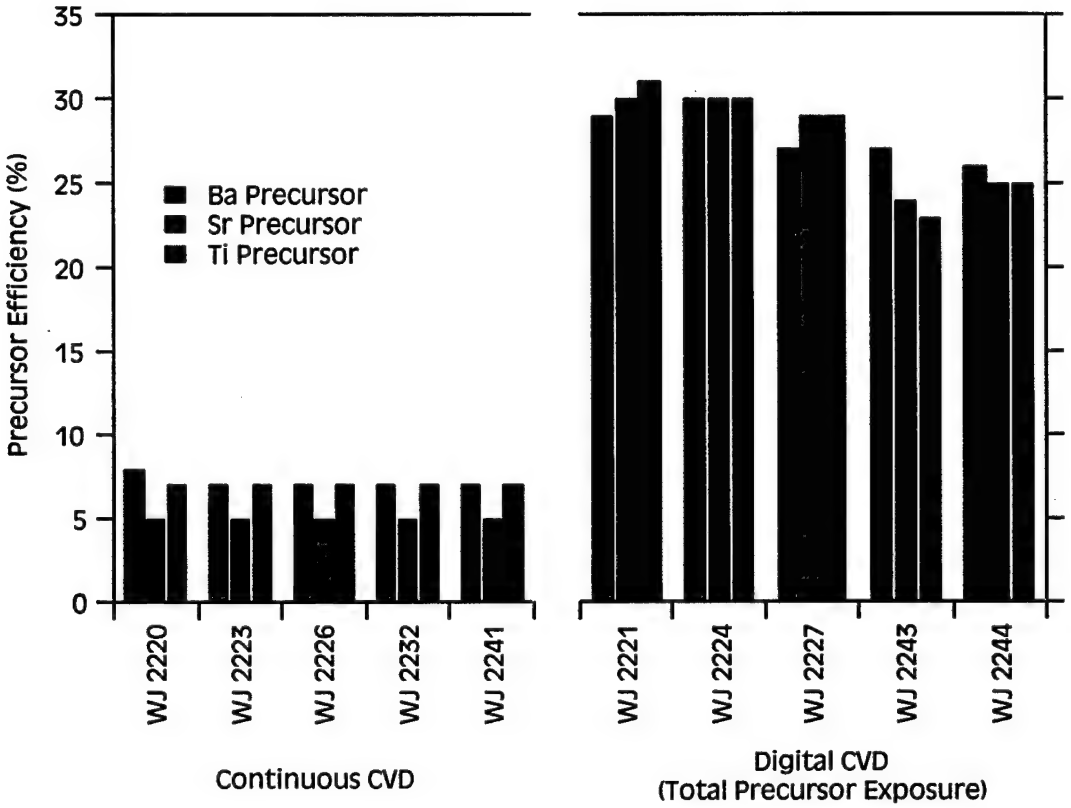



Figure 11. Precursor Efficiencies as a function of run number for both the continuous and digital process.

**Increased Crystallinity at Lower Temperatures.**

Figure 12 shows a series of θ/2θ X-ray diffraction scans that illustrate the improved crystallinity. The bottom panel is data from a film grown using the continuous CVD process at 560°C, and there are no crystalline BST peaks present. The top panel shows data from a film grown at the same temperature but with the digital process, and crystalline BST peaks are present, one of which is pointed out in the graph. As the temperature was decreased, the crystalline peaks are still seen at 520 °C, and there are even some small peaks at 500 °C.

**Improved Thickness Uniformity**

Figure 13 shows that the digital CVD process has also resulted in increased thickness uniformity. The striped bars on the left of the graph are the thickness that were measured on films that were deposited on the left and right side of the substrate heater. These can be compared with films grown in identical positions using the continuous CVD process. Substrates

are ¼ of a four-inch wafer in size, and separated by approximately 1-2 inches. For films grown digitally, there is less than a 1.7% difference in thickness, where as for films grown with the continuous method there is a 20% difference.

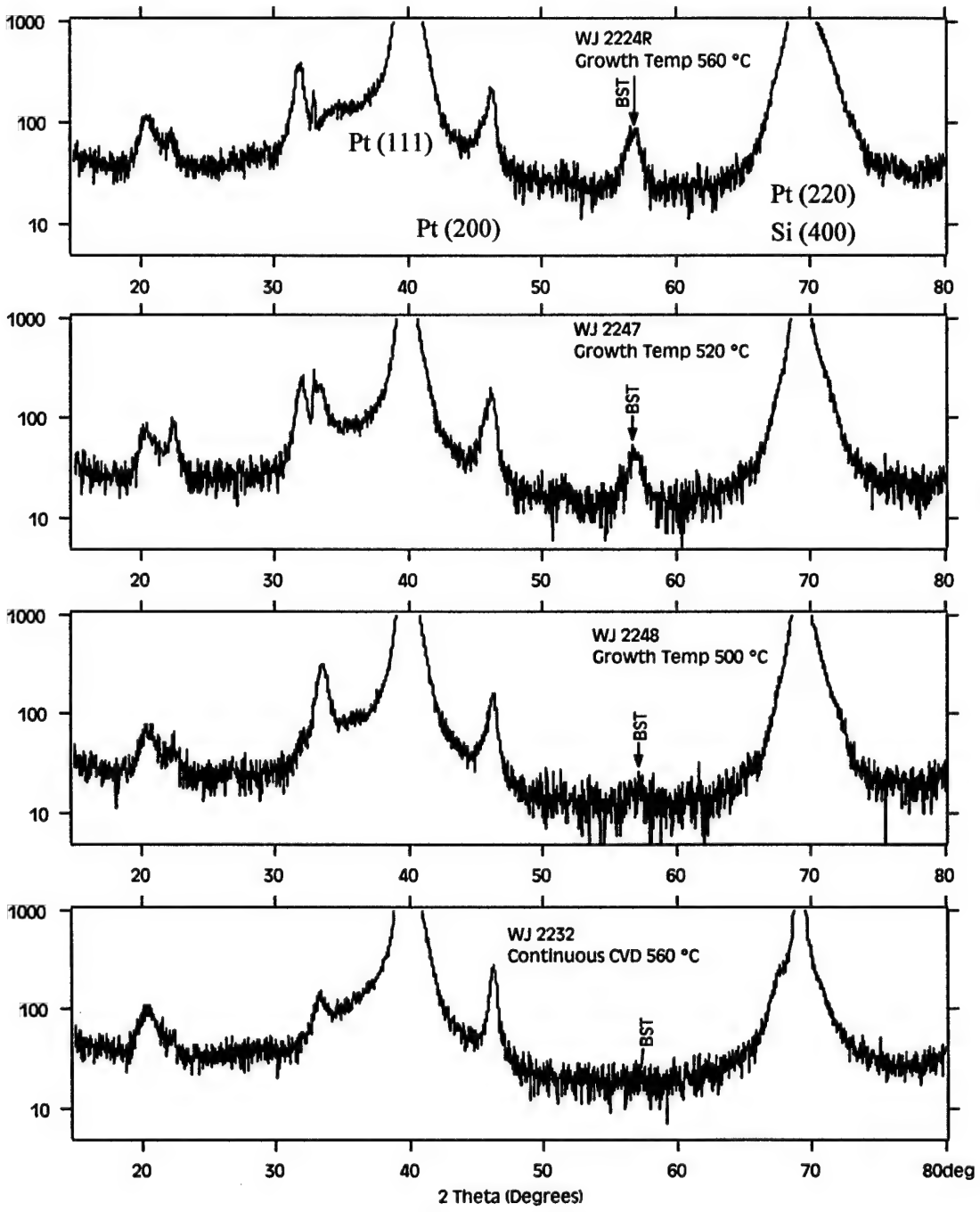



Figure 12. X-ray diffraction patterns as a function of deposition process for the digital CVD process

**Ozone Processing**

An important motivation for the development of the digital CVD process was the desire to use more aggressive oxidation methods without detrimental gas phase reaction between the precursors and the oxidizers. To illustrate the effect of gas phase reactions, Figure 14 shows the effect of ozone on the incorporation efficiency of the Ba, Sr and Ti precursors in a continuous MOCVD process. This data was collected using a hot wall inverted quartz research reactor, at a deposition temperature of 470 °C. This low temperature was used in order to minimize the amount of gas phase reactions that might occur due to gas heating from the substrate. As the amount of ozone was increased, the efficiency of the Ba and Sr precursors decreased and the efficiency of the Ti precursor increased. In addition, particulate formation was observed on the sidewalls of the reactor, indicating that there was substantial gas phase reactions occurring between the ozone and precursor in the continuous process.

Figure 15 shows the affect of ozone on the incorporation efficiency of the Ba, Sr and Ti precursors using the digital CVD process. This data was collected in the WJ deposition system at a temperature of 590 °C, Figure 16, at conditions listed in Table 10. As the amount of ozone is increased, there is almost no effect on the Ti efficiency, and only a small effect on the Ba and Sr efficiencies, up to a partial pressure of ozone of nearly 30 mTorr. This is an order of magnitude higher partial pressure of ozone than was used in the continuous CVD process discussed above. We suspect that the small effect of ozone concentration on the Ba and Sr efficiency is due to residual precursor that is not being completely removed during the purging pulse. This is primarily a function of reactor design, and it is expected that this could be minimized in future hardware configurations.

Room temperature electrical measurements were performed on these films as a function of ozone wt %, and is shown in

Table 11. Each film exhibited the characteristic dielectric constant vs bias behavior, with a maximum dielectric constant of 126 for the film grown with 12 wt% ozone. The addition of ozone resulted in substantial improvements of the dielectric constants at these compositions and growth temperatures. These films, grown at 590 °C, were about 600 Å thick, which results in a maximum charge storage density 22.6 $fF/\mu m^2$ for the film grown with 12 wt% ozone. Leakage current densities of ~$5x10^{-3}$ $A/cm^2$ @ 1V were measured for all films.

These experiments demonstrate the efficacy of the digital CVD process in minimizing gas phase precursor reactions. They have also demonstrated an effective strategy for the use of a more aggressive oxidizer such as ozone. The electrical performance of films deposited with the digital CVD process in the WJ reactor, however, did not achieve the same level as films deposited via the conventional process in the Varian Reactor. Because we have observed substantial improvements in the electrical performance of BST grown by the conventional CVD process in moving from the WJ to the Varian reactor, we believe that the lower electrical performance

observed here is due to differences in the reactors rather than an inherent limitation of the Digital CVD process. These differences include the use of a vacuum load lock and improved composition control found in the Varian system. Additionally, substantial effort has been devoted by the DRAM community in optimizing the electrode interfaces for the conventional process. Such optimization would be needed for the digital process in order to match those results.

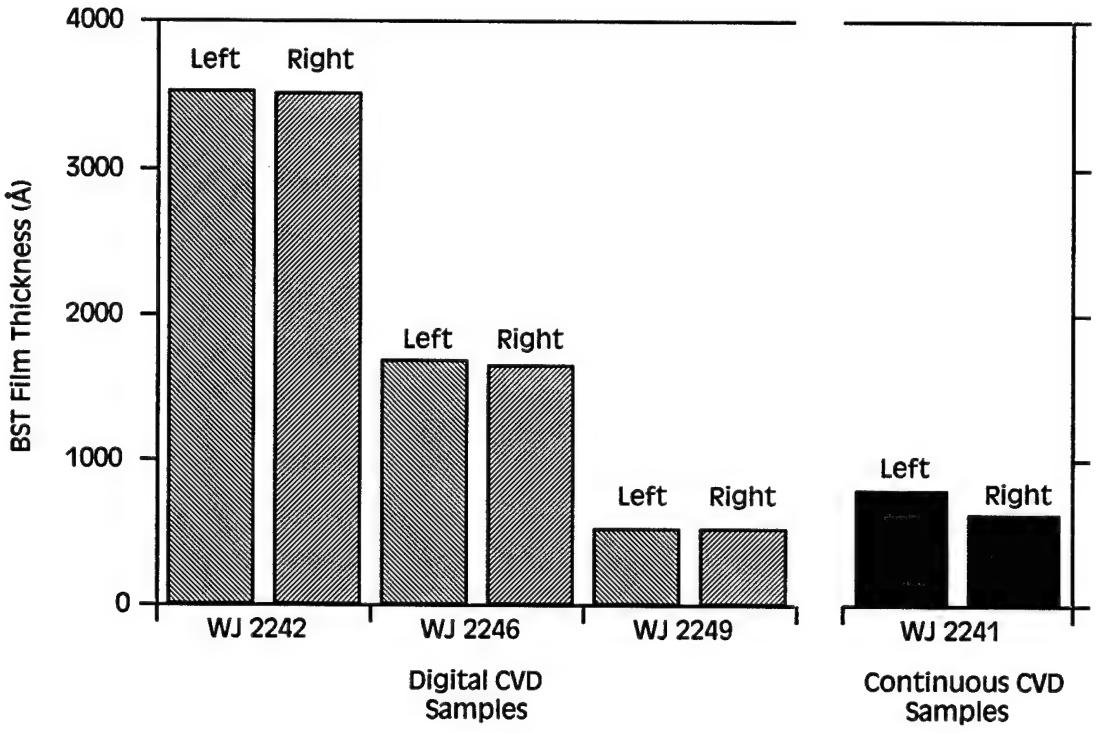



Figure 13. Thickness variation as a function of position on the substrate holder

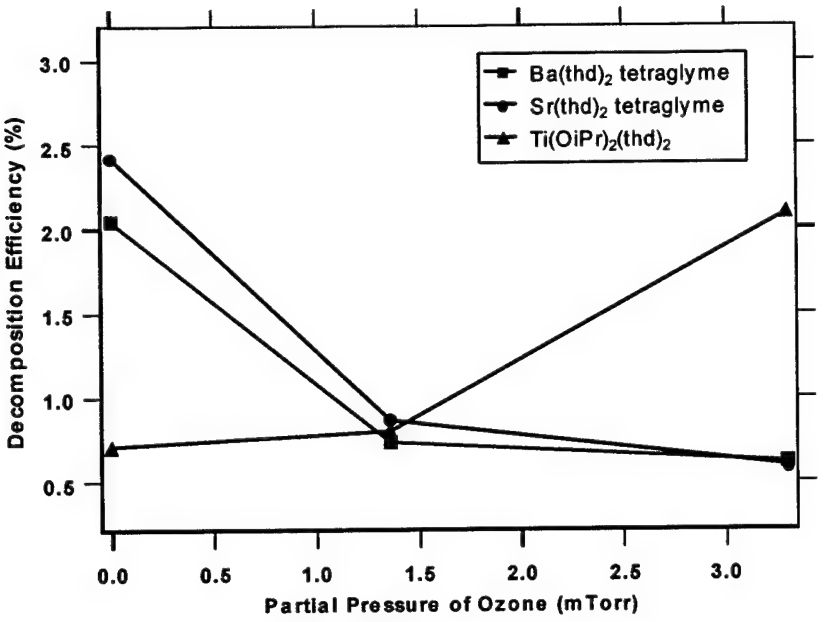



Figure 14. The effect of ozone on the precursor efficiencies in the continuous CVD process.

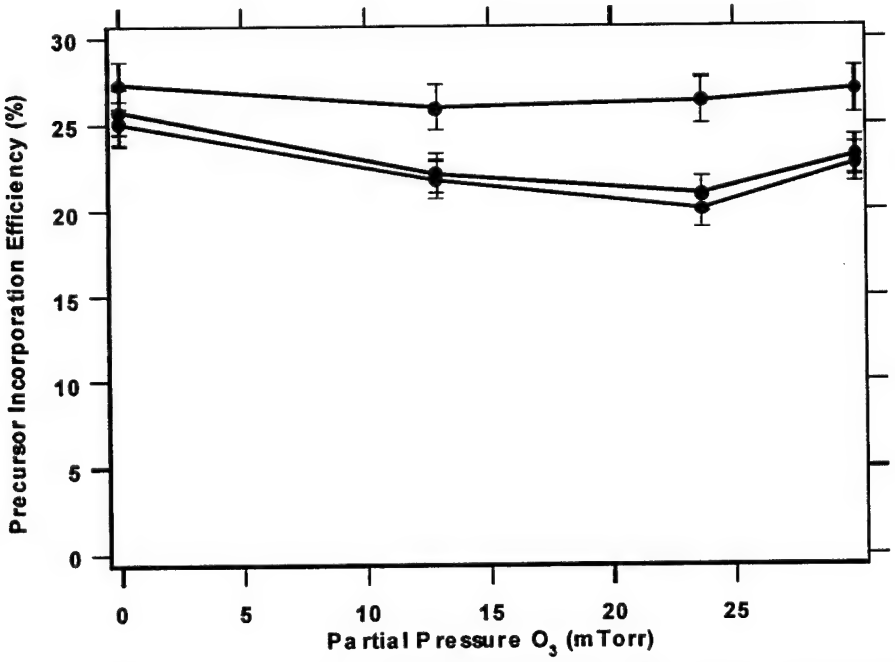



Figure 15. The effect of ozone on the precursor efficiencies in the Digital CVD process

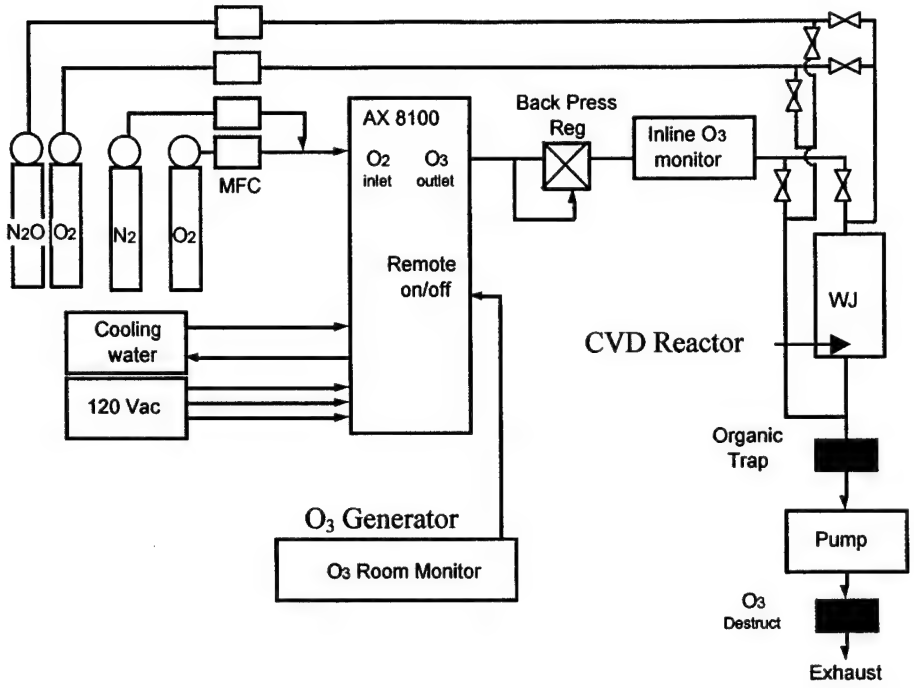



Figure 16. Schematic of the MOCVD system, which incorporates the use of a Astex model AX8100 Ozone generator.

Table 10. Typical Growth Parameter used to date in Digital CVD processing of BST using ozone

| **Growth Parameter** | **Range** |
|---|---|
| Precursor Pulse Width, T1 | 7-25 s |
| Ar Purge Pulse Width, T2 | 7-14 s |
| Oxidizer Pulse Width, T3 | 7-14 s |
| Ar Purge Pulse Width, T4 | 7-14 s |
| Number of cycles | 10-20 |
| Oxygen flow rate | 500 sccm |
| Wt % $O_3$ in $O_2$ | 0-15% |
| Growth temperature | 420-600 °C |
| Liquid Precursor Flow rate | 0.08 ml/min |

Table 11. Electrical Characterization of films grown with and with Ozone with the Digital CVD process

| **Sample#** | **Wt % $O_3$** | **Thickness (angstroms)** | **Capacitance (pF)** | **Storage Density (fF/μm²)** | **Dielectric Constant** |
|---|---|---|---|---|---|
| WJ 2482 | 0 | 614 | 5.37e2 | 8.1 | 47 |
| WJ 2481 | 5 | 594 | 1.34e3 | 20.2 | 113 |
| WJ 2487 | 12 | 592 | 1.50e3 | 22.6 | 126 |

## Amorphous Mixed Oxide Thin Film Development

For the IC integration compatibility assessment, we have relied on input from Raytheon, the primary end-user of the cryogenic IRFPA process. As described above, our initial goal was to develop an *in situ* process with a temperature of 580°C or less, and this goal was achieved. Through communications and interactions over the coarse of program, however, Raytheon informed us that they would be significantly more interested in processes with a deposition temperature of less than 450 °C, and preferably less than 400 °C. This is governed by their desire to stay beneath the temperature of the last forming-gas anneal in their CMOS fabrication flow.

In order to reduce the thermal budget to meet these new requirements, we began the investigation of two novel processing pathways to produce high dielectric integrating capacitors: 1) low temperature-high pressure BST deposition, with and without RTA, and 2) amorphous mixed oxide thin film deposition.

### High Pressure, Low Temperature Processing of BST Films

In the course of depositing of mixed oxide (see ff.) it was observed that high growth pressures increased growth rates and efficiencies at low deposition temperatures, allowing reasonable film growth rates as low as 350 °C. The first pathway we have taken to achieve lower processing temperatures is the investigation of low-temperature high-pressure conditions for the deposition of amorphous BST. One of the primary hurdles in lowering the deposition temperature of BST is that the precursor deposition efficiency falls off with decreasing temperature. In work on other precursor systems at ATMI it was discovered that their deposition efficiency could be maintained at lower temperatures by increasing the deposition pressure. This was a relatively unexplored region of the deposition space for BST processes, so the first step along this pathway was to investigate this space via a designed experiment. In this experiment, the variables were Temperature and Pressure, and the measured responses were the precursor efficiencies. The solution flow rate, 0.08ml/min, and the composition (Ba 0.06 molar, Sr 0.06 molar, and Ti 0.35 molar) were held constant.

Figure 17,

Figure 18, and Figure 19 are plots of the efficiencies for the Ba, Sr and Ti sources respectively, and show that there is a strong effect of both temperature and pressure in this regime, with efficiencies increasing with both increasing temperature and pressure. Although the increase with temperature is expected, the increase with pressure is contrary to the behavior at the conventional temperatures >640 °C, where higher pressures lead to a decrease in efficiency.

Figure 20 consists of plots of the screening model analysis and confirm that both temperature and pressure have statistically significant effects on the efficiency. Of the three, the Ti efficiency is the least affected by the deposition pressure.

These results were used to design a growth experiments in a load-locked tool, similar to the Varian Oxides tool of Figure 1. Efficiency around 10-12% is typical for a low pressure reactor in which one is trying to obtain good BST uniformity (efficiencies much greater than this

tend to cause stronger thickness and stoichiometry gradients in thin films). Figure 21 shows efficiency vs. growth temperature in the pressure range we use for normal, high temperature MOCVD growth of BST, 0.7 torr.

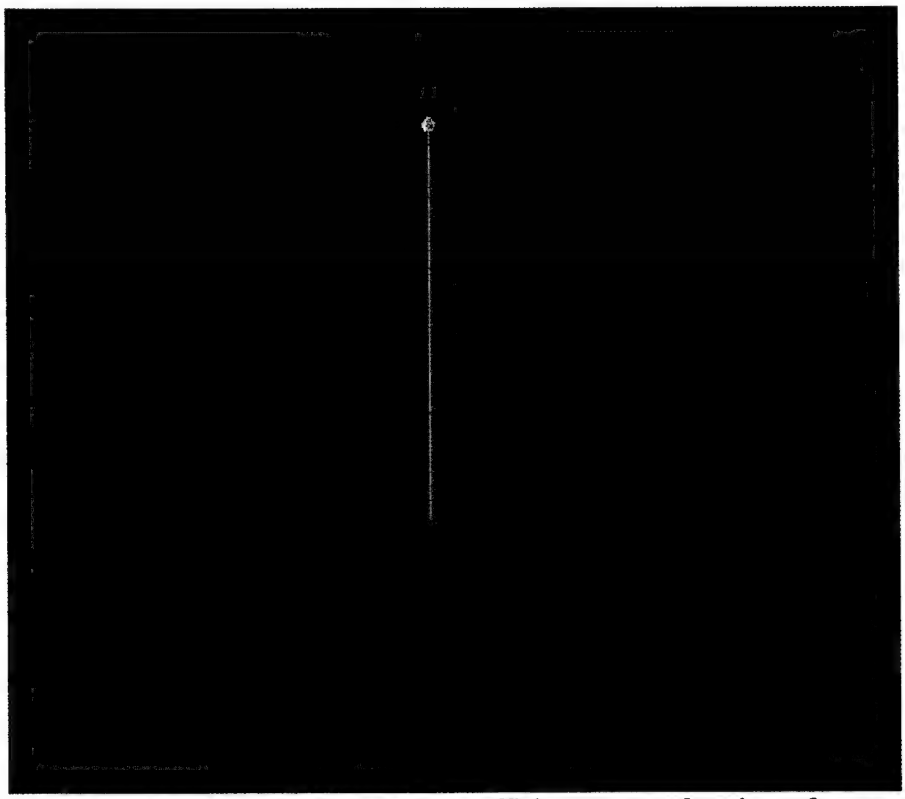


Figure 17 Barium precursor ($Ba(thd)_2$pmdeta) efficiency as a function of temperature and pressure.

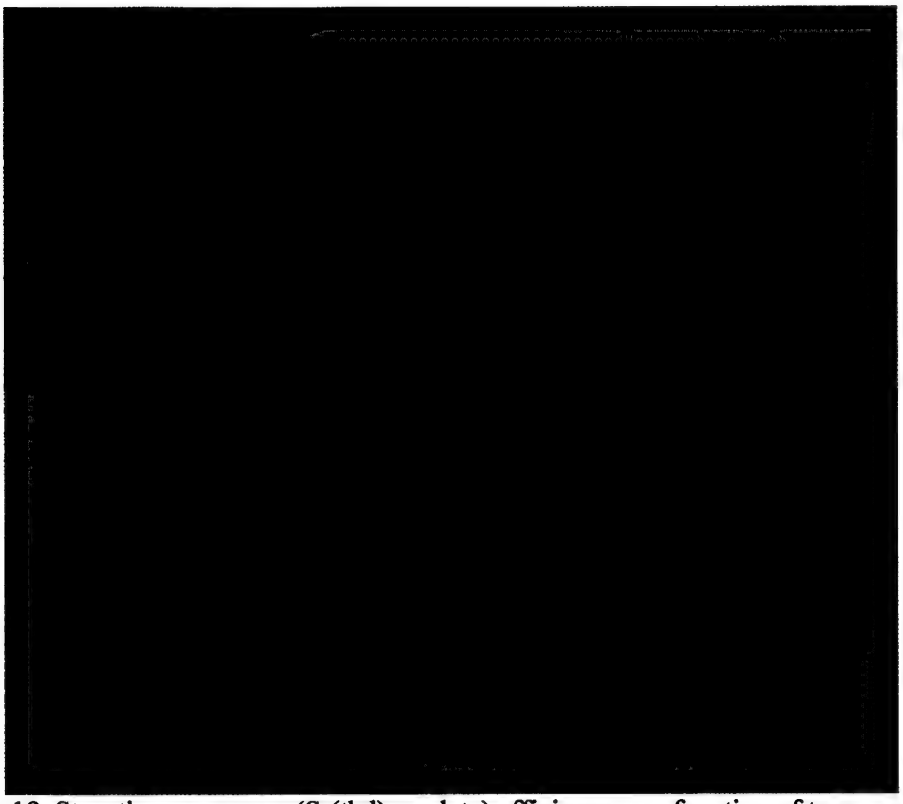


Figure 18 Strontium precursor ($Sr(thd)_2$pmdeta) efficiency as a function of temp and pres.

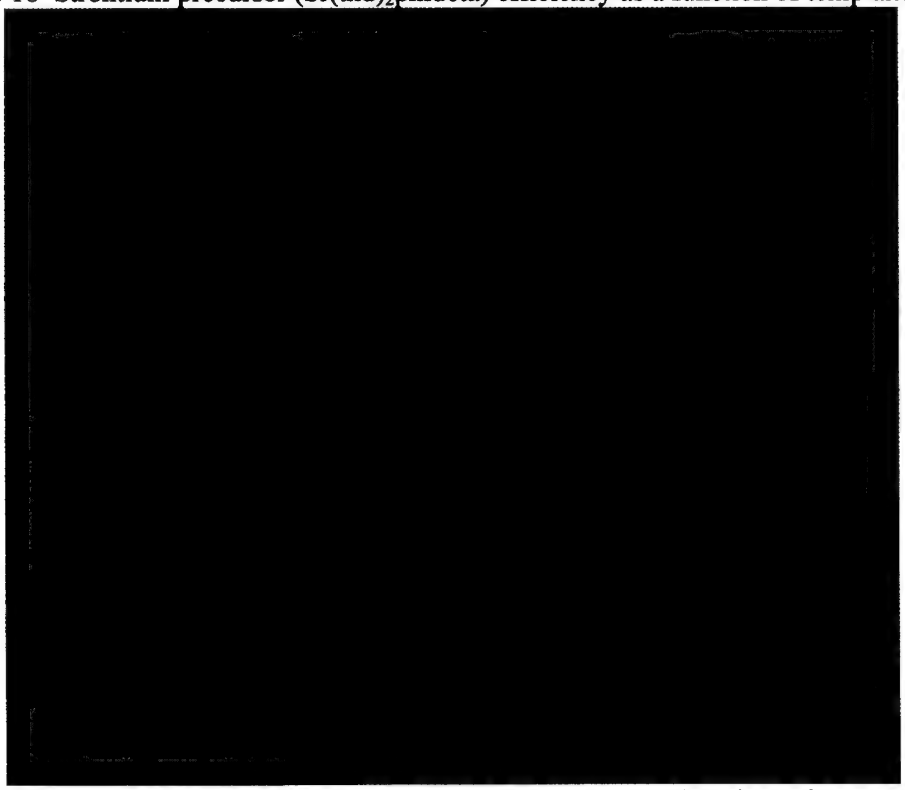


Figure 19 Titanium precursor ($Ti(OiPr)_2$ ($thd_2$) efficiency as a function of temperature and pressure.

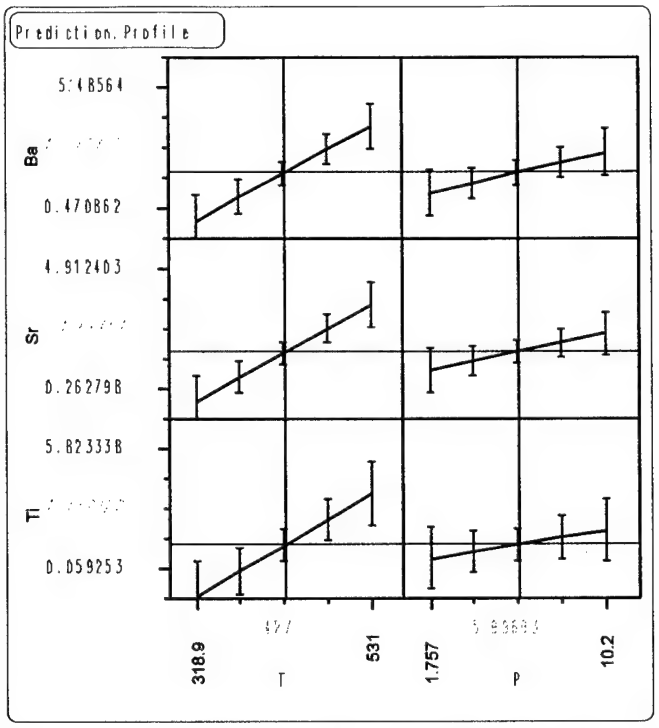



Figure 20 Result of a screening model fit analysis for the data shown in the previous figures above. This analysis confirms the significance of the effect of temperature and pressure on precursor decomposition efficiency

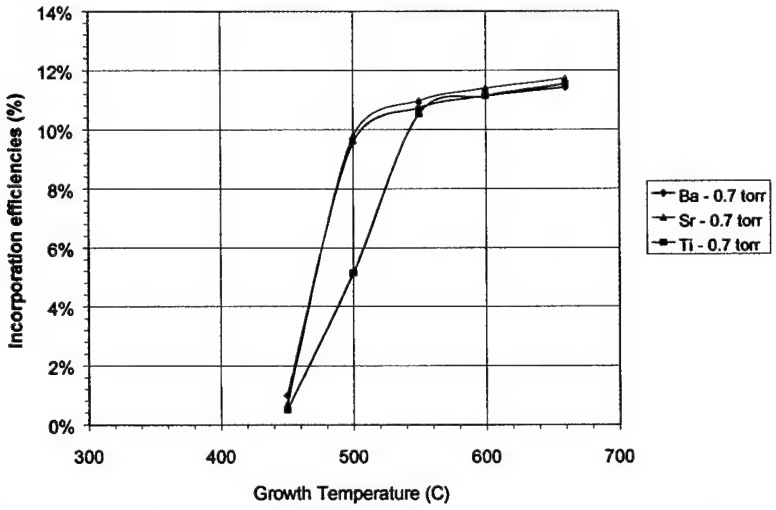



Figure 21. BST precursor utilization efficiency vs. growth temperature at 0.7 torr. Above 500 °C, relatively flat efficiencies are seen, making stoichiometry control easy in this regime, but between 400 and 500 °C efficiencies are a strong function of temperature.

In the surface reaction controlled growth regime which is active below 500 °C in Figure 21, efficiencies are very strongly dependent on growth temperature. As expected from the nature of the precursors used, efficiencies of Ba and Sr track each other quite well, but Ti is significantly

different. This makes stoichiometry control across a wafer challenging, since even minor temperature variations cause significant changes in film stoichiometry, especially in the ratio of Group II elements to Ti, which has a big effect on electrical properties. Even when producing amorphous films and annealing them for crystallinity, as we plan to do in this program, this can be a concern. A somewhat less steep efficiency profile, such as that seen in Figure 22, would be desirable.

While significant efficiency dependence on growth temperature is still seen below 500 °C in Figure 22, the slope of the curve is gentler, making film stoichiometry somewhat less dependent on growth temperature. More importantly, efficiencies of the Group II elements are still above 2% at 400 °C, and Ti efficiency is almost 1%. These are more than double the efficiencies seen at 0.7 torr, and indicate that BST films can still be grown at these low temperatures. Growth rates are very low, though, so the majority of films discussed from this point on were grown at 450 °C.

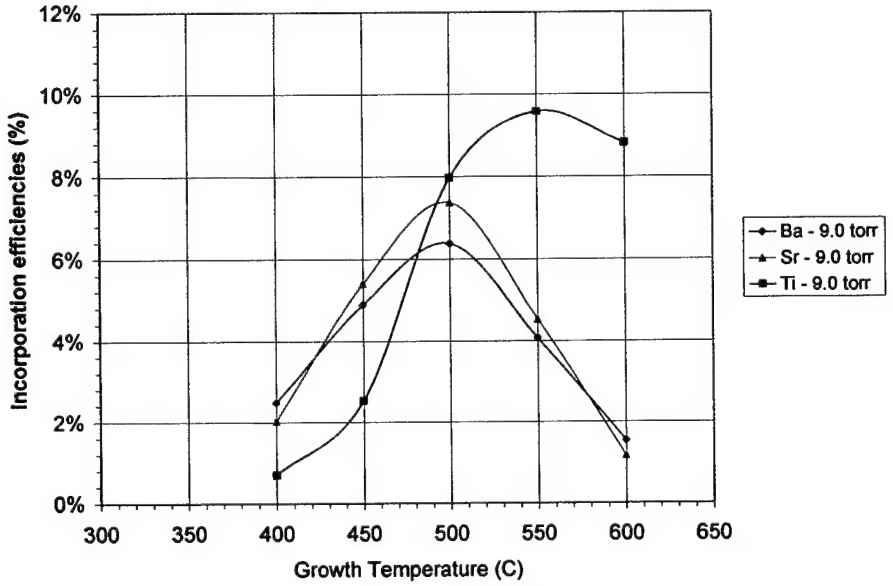



Figure 22. BST precursor utilization efficiency vs. growth temperature at 9.0 torr. Dependence of efficiency on temperature is somewhat lower than that seen at 0.7 torr, making stoichiometry control in the film easier, and absolute efficiencies seen at 400 °C are more than double those at 0.7 torr.

**Physical Characterization**

We began by examining the x-ray diffraction (XRD) spectra of these films in order to determine the degree of crystallinity of the BST at different growth temperatures. In normal perovskite BST films grown on Pt by MOCVD, the (100) crystallographic orientation is predominant. As Figure 23 shows, temperatures above 600 °C are needed to achieve any appreciable degree of crystallinity in the films grown in our standard process at 0.7 torr. Some

crystallinity is seen at 600 and 550 °C, and essentially none at 500 °C, where films seem to be amorphous.

While the lower temperature films seem to be amorphous or very fine grained microcrystalline, note that as discussed in previous reports, the films grown below 600 °C are not necessarily balanced in the 50:50 Group II:Ti ratio needed for perovskite films because of the significant changes in relative precursor efficiency. We have found in previous experiments, for example, that excesses of Ti over about 15% have a strong tendency to drive films amorphous even when grown at high temperatures. Specifically, the films in Figure 23 grown at temperatures of 550 °C and above are about 58% Ti, while those grown at 450 and 500 °C are about 43% Ti.

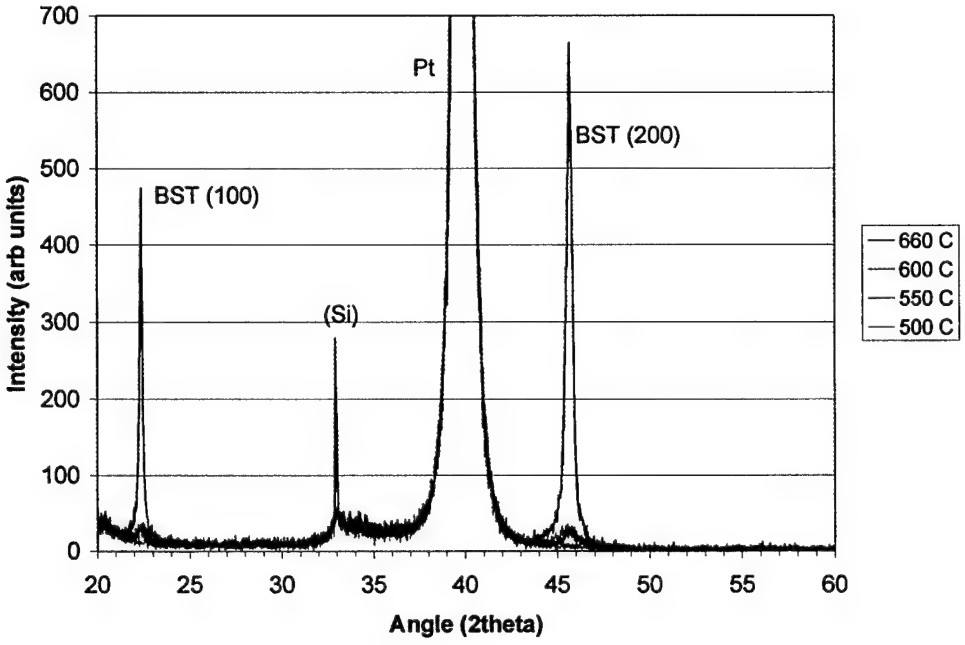



Figure 23. X-Ray diffraction spectra of BST films grown on $Pt/SiO_2/Si$ at 0.7 torr and various deposition temperatures, showing (100) orientation. Significant crystallinity is only seen at 660 °C, though small peaks are visible at 550 and 600 °C.

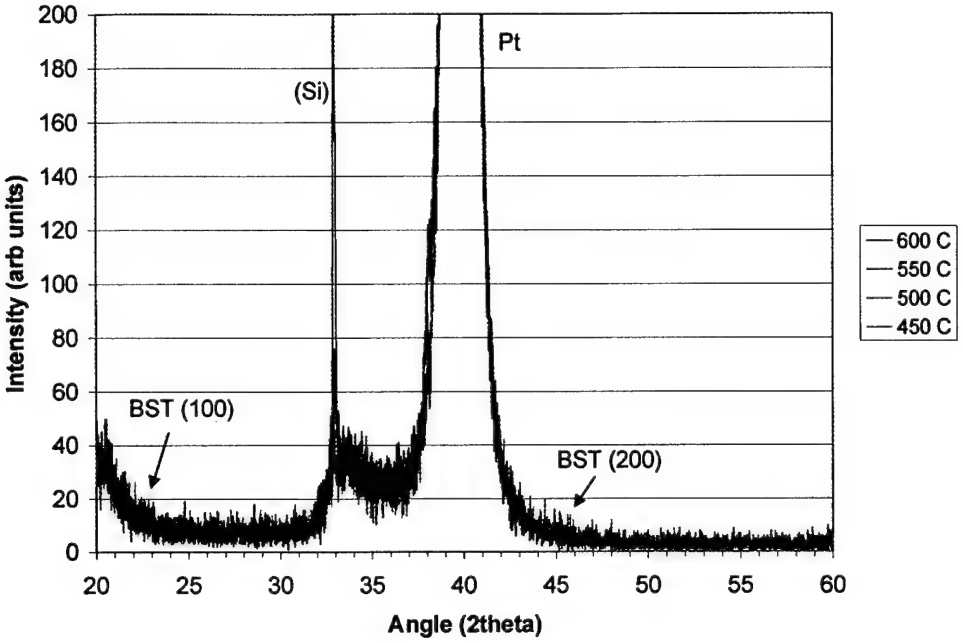



Figure 24. X-Ray diffraction spectra of BST films grown on $Pt/SiO_2/Si$ at 9.0 torr and various deposition temperatures, showing amorphous films under all conditions. Note that stoichiometry is significantly off from perovskite in all films (see above), which may impact crystallinity as well.

## Rapid Thermal Annealing Process Experiments

When reactor pressure is higher, 9.0 torr, XRD spectra show only amorphous BST films to be present. This could be due to a combination of low growth temperatures and significantly altered stoichiometry from the optimal perovskite ratio, as discussed above. More films were then grown with stoichiometry compensation to achieve the desirable 50-55% Ti content used for high storage density BST capacitors, and rapid thermal anneals (RTA) were performed on the films. Even at temperatures well above that which could be tolerated by the Si devices under the BST films, little change in crystallinity was seen. This is shown in Figure 25 where an XRD pattern for an as-grown film produced at a substrate temperature of 450 °C is compared to that seen after a 1 minute, 1000 °C RTA in $N_2$ on the same film.

### Electrical Properties

We then examined the possibility of using RTA post-processing to improve electrical properties of the films, in particular increasing the dielectric constant of the low ε as-grown films. Interestingly, even though virtually no change is visible in XRD with RTA processing of the films, some improvement does take place in electrical properties. In order to examine this, we selected a sample with representative properties and measured sections of it without any RTA and with RTA processing at several different temperatures. It is important to remember that the goal of the program is to make storage capacitors with high charge storage densities without a high

thermal load on the Si circuitry beneath. In general, it is desirable to keep processing temperature to below 500 °C, with 500-550 °C considered a maximum. Table 12 shows the samples and RTA processing conditions used for these experiments.

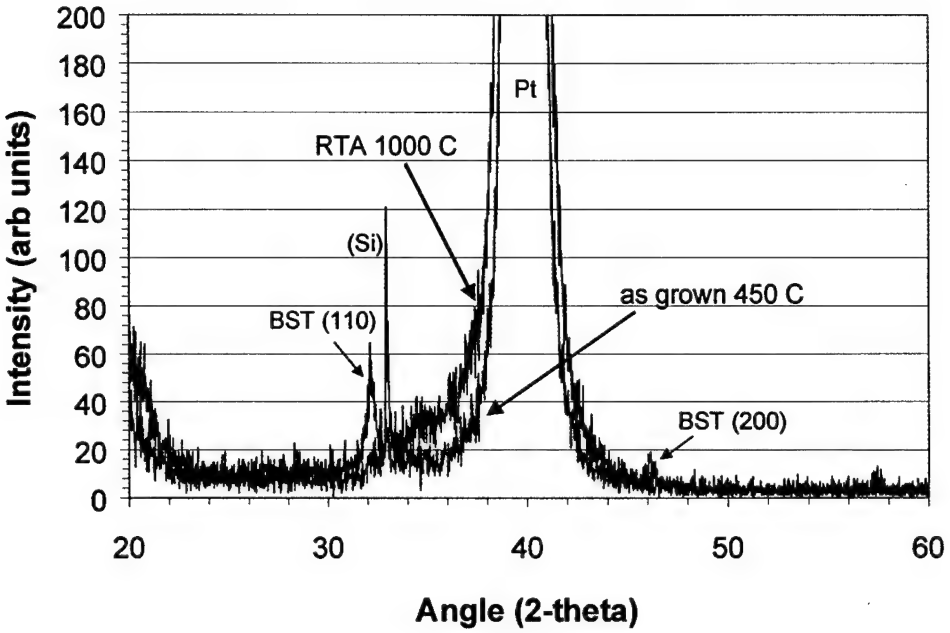



Figure 25. XRD spectra for 631 Å BST film grown at 450 °C, before and after 1000 °C, 1 minute RTA. Despite the high anneal temperature used, little change in crystallinity is seen, with final peak intensities at least an order of magnitude below that seen in an equivalent film grown at 660 °C.

Table 12. Description of RTA processing of samples.

| Sample # | RTA temperature | Time of RTA |
|---|---|---|
| AV 220.CC 3-4 | N/A | 1 minute |
| AV 220.BB 1 | 450 °C | " |
| AV 220.BB 2 | 500 °C | " |
| AV 220.BB 3 | 550 °C | " |
| AV 220.BB 4 | 600 °C | " |
| AV 220.CC 1-2 | 1000 °C | " |

For a control, one sample was not RTA processed at all, while another sample was processed at a much higher temperature than would be allowed for this process, 1000 °C, in order to explore the ultimate boundaries of RTA utility for modification of low temperature BST properties. The BST film used for this set of experiments was grown at 450 °C, and was 631 Å thick. Figure 26 shows the results of electrical measurements on these samples. Measurements

were either made between top electrodes, using probes, or in a 40-pin package with wire bonds to top electrodes on BST (as described elsewhere).

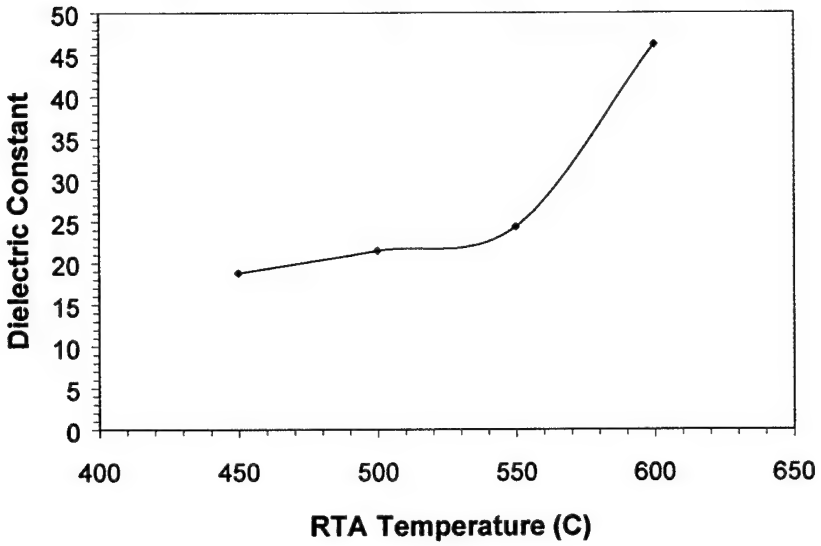



Figure 26. Dielectric constant vs. RTA temperature, showing that little gain is seen with RTAs up to 550 °C, though some improvement takes place with an RTA at 600 °C. A dielectric constant over 400 can be achieved with RTA at 1000 °C (not shown), but this is far too high of a processing temperature for this application.

We found that with RTA processing up to 550 °C, considered the approximate upper limit of an acceptable manufacturing process for the IR detectors in which these storage capacitors will be used, virtually no improvement in dielectric constant was seen, as shown in Figure 26. RTA at 600 °C improves dielectric constant somewhat, going from about 24 to 46, almost a 2x improvement, while RTA at 1000 °C (not shown on plot) improves dielectric constant by almost another order of magnitude to 446, though this would clearly be far beyond the thermal load acceptable for the application.

After conventionally grown BST has top electrodes deposited, it is normal practice to carry out an anneal of the electroded devices at approximately 550 °C for one half hour. This is found to reduce leakage and improve electrical properties, as well as increase sample-to-sample uniformity, in the BST thin films. We have also found that an RTA at this temperature for one minute achieves approximately the same effect. Therefore after preliminary electrical measurements on the samples, we performed a 450 °C, one minute RTA on them. No significant change in dielectric constant was seen.

## Cryogenic Measurements of Amorphous and RTA BST

In order to carry out the cryogenic measurements made on these samples we have made use of an outside vendor which specializes in unusual wire bonding and packaging of semiconductor samples, American Dicing of Syracuse, NY. Gold wire was used to wire bond to the top electrodes, which were 1000 Å thick Pt dots patterned by e-beam evaporation through a shadow mask, and the samples were inserted into a standard 40-pin package for immersion in liquid nitrogen.

We first compared dielectric constants at room temperature and 77 K, finding that there was only about a 5% decrease in each case at 77 K from that shown earlier in the plot of room temperature dielectric constant. We then examined the effect of cryogenic temperatures on leakage, which can be correlated to breakdown voltage. Results are shown in Figure 27 to Figure 30.

In each case leakage is considerably lower in these films at cryogenic temperatures than at room temperature, showing their suitability for the integrating capacitor application. As expected, losses also decreased from a range of 1-2% down to about 0.6% for these capacitors. It is also interesting to compare the 77 K properties for each of these films directly as a function of RTA temperature, as in Figure 31, below.

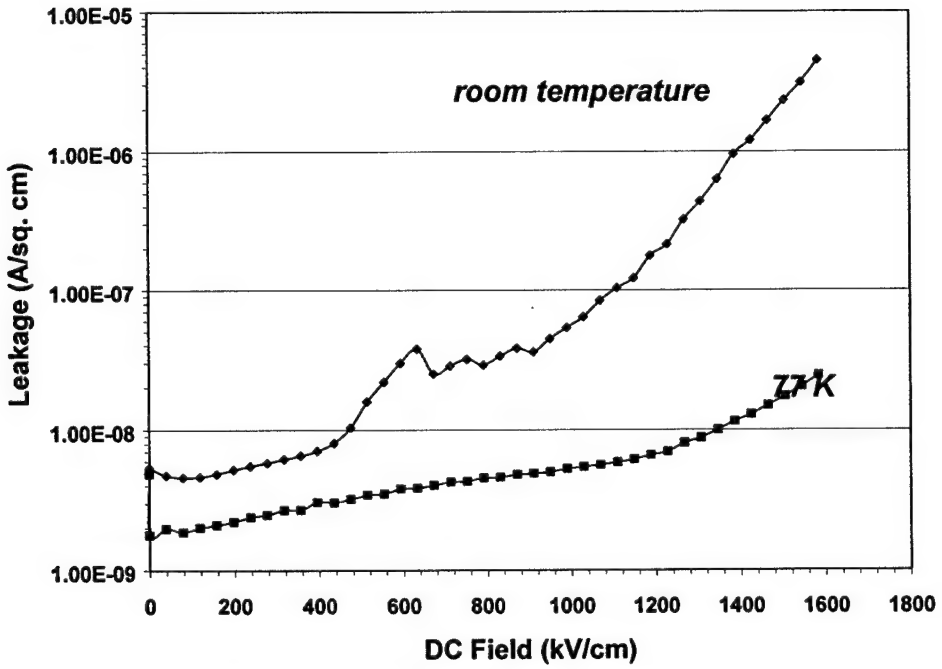



Figure 27. Leakage vs. DC bias for a 631 Å thick film grown at 450 °C and RTA processed at 450 °C, showing that leakage is significantly improved when the capacitor is measured at cryogenic temperatures.

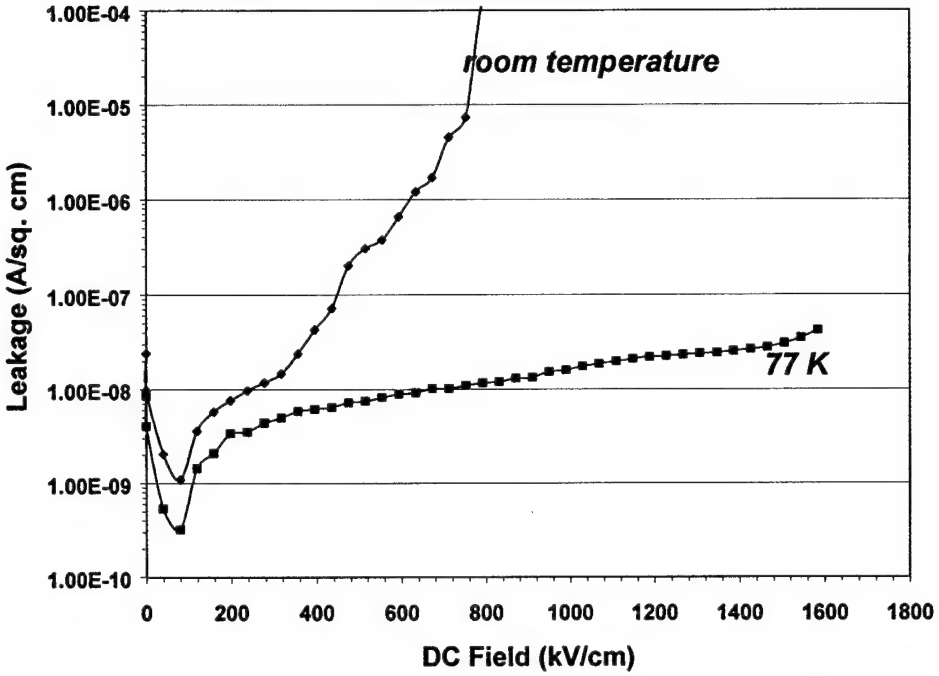



Figure 28. Leakage vs. DC bias for a 631 Å thick film grown at 450 °C and RTA processed at 500 °C, showing that leakage is significantly improved when the capacitor is measured at cryogenic temperatures.

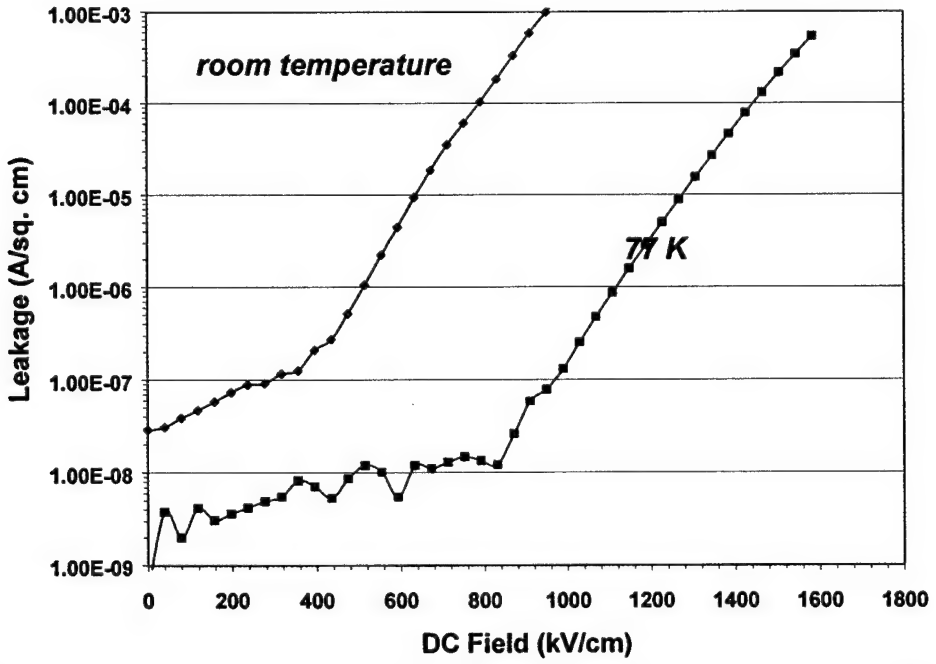



Figure 29. Leakage vs. DC bias for a 631 Å thick film grown at 450 °C and RTA processed at 550 °C, showing that leakage is significantly improved when the capacitor is measured at cryogenic temperatures.

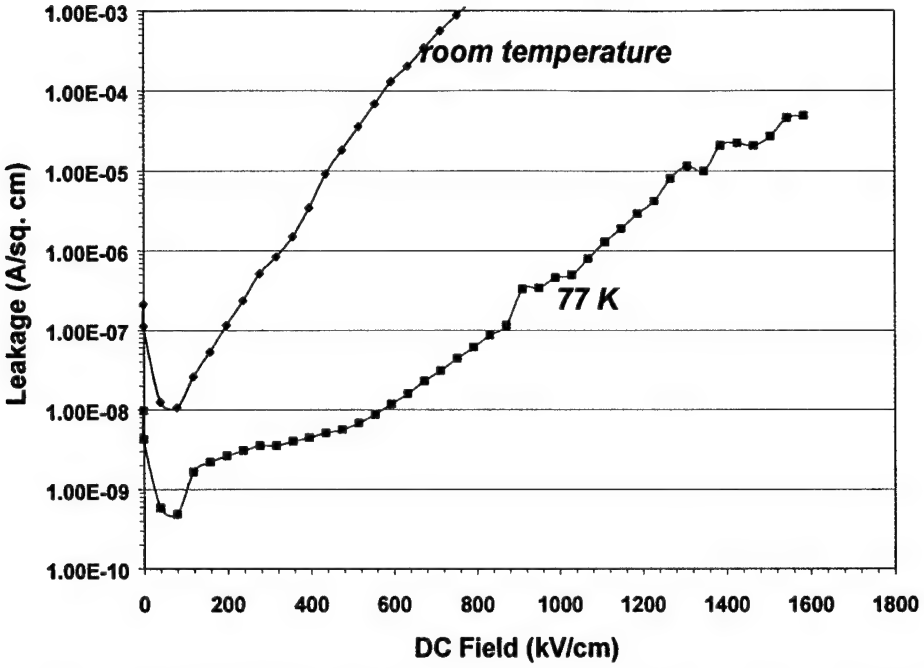



Figure 30. Leakage vs. DC bias for a 631 Å thick film grown at 450 °C and RTA processed at 600 °C, showing that leakage is significantly improved when the capacitor is measured at cryogenic temperatures.

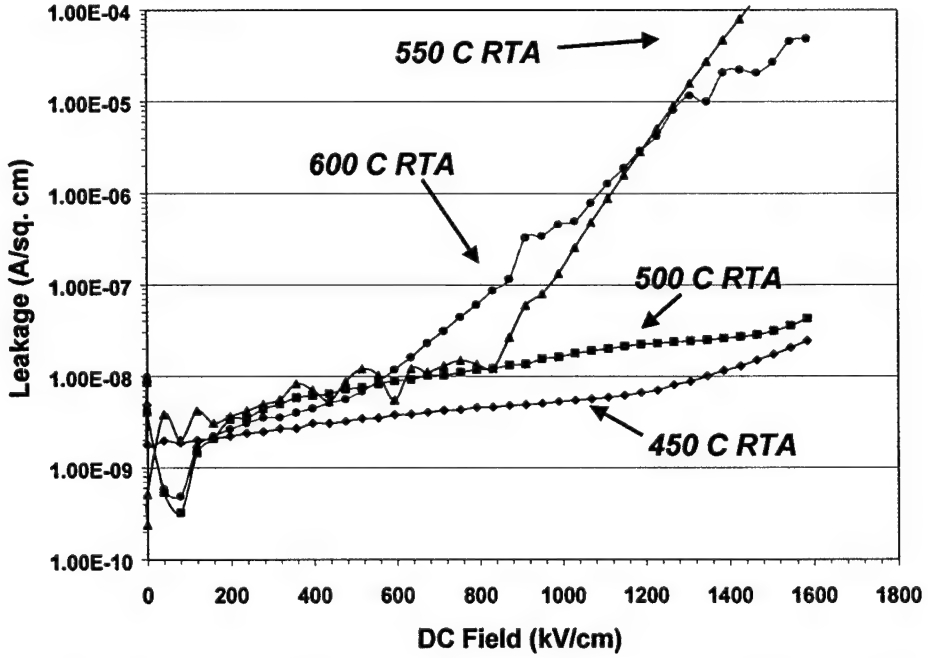



Figure 31. Comparison of cryogenic leakage measurements on films with different RTA conditions, showing that 77 K leakage increases significantly with RTAs over 500 °C.

It can be seen in Figure 31 that 77 K leakage increases significantly with RTAs over 500 °C. Since the dielectric constant is relatively flat (~20) with these low RTA temperatures, C/A

may actually be higher with films which undergo lower temperature processing. This is encouraging for the envisioned application, which requires low total thermal loads on devices since the integrating capacitor is deposited and fabricated after much of the rest of the semiconductor device is produced.

In order to examine this possibility, we carried out calculations on projected C/A values for these films. Setting a leakage criteria of $10^{-8}$ A/cm$^2$ for breakdown (note that in Figure 31 leakage increases rapidly at about this point for the films which had higher temperature RTAs) in order to set appropriate film thicknesses for each operation voltage and using the dielectric constant values shown earlier, we can calculate estimated C/A values for these capacitors. This calculation assumes operation at the breakdown criteria, which may be aggressive, and that breakdown properties do not vary with film thickness; a more extensive development program would be needed to verify these assumptions. Results are shown in Figure 32; note that the C/A values shown may be optimistic if more conservative voltage operation is assumed..

It can be seen in Figure 32 that there are interesting tradeoffs which appear in C/A values. The highest values are those for the lowest (450 °C) and highest (600 °C) RTAs, due to high breakdown voltage for the lowest RTA temperature and high dielectric constant for the high temperature RTA. Intermediate RTA temperatures, meanwhile, have a poor combination of breakdown voltage. It should be noted that a 600 °C RTA is probably unfeasible for the desired application, so low temperature RTAs would be best.

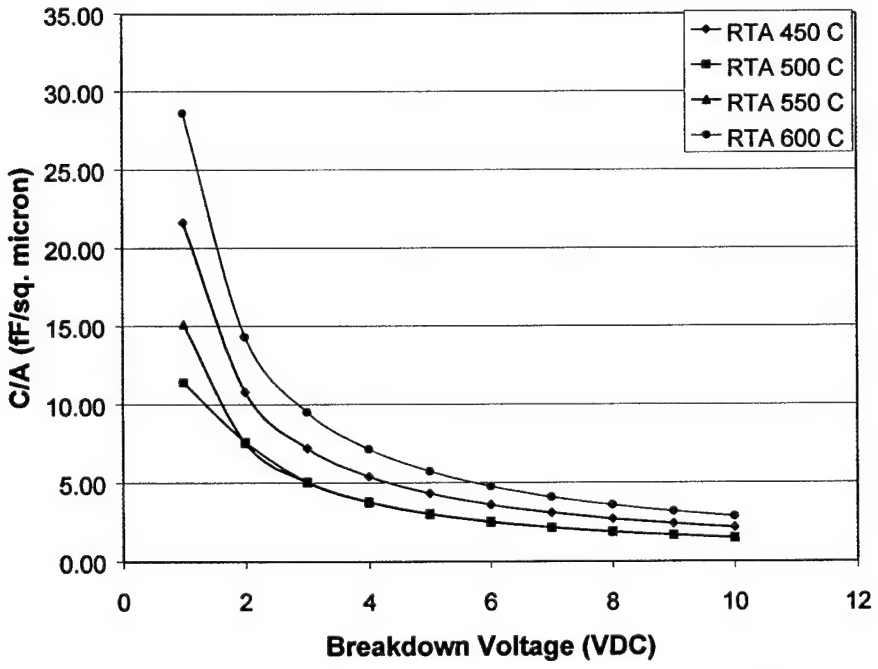



Figure 32. Calculated C/A values for BST films, based on operation voltage at breakdown (breakdown criteria used was $10^{-8}$ A/cm$^2$ leakage). The highest and lowest temperature RTAs give better performance, though 600 °C is expected to be too high for the candidate operation.

## Amorphous mixed oxide dielectric thin films

The second pathway we have taken to achieve lower processing temperatures is the investigation of amorphous mixed oxide thin films. Measurement of amorphous mixed oxide thin films indicated that this material could provide a low temperature route to a high k material suitable for integrated circuits. We performed two sets of experiments to explore the potential of this materials system for the IRFPA application. The first set of experiments examined the dielectric properties over a region of composition space, and the second experiment was designed to examine the dielectric properties as a function of film thickness and deposition temperature at a single composition, which was identified as preferable in the broad composition scan of the first experiment. Finally, various thicknesses of these samples were packaged and measured electrically at cryogenic temperatures.

### Composition scan

*Electrical measurements*

Top electrodes were formed by e-beam evaporation of Pt through a shadow mask. The capacitance (and loss) increases slightly as the bias voltage is increased as shown in Figure 33, but the change is less than 0.5%. When the same sample was measured at Raytheon, it was found to have a capacitance density of 9.5 $fF/\mu m^2$ at 77K and 10.0 $fF/\mu m^2$ at 296K, which is within experimental error. The temperature dependence of the dielectric constant is smaller in the amorphous mixed oxide film than it is for the crystalline BST films, ranging from 5 to 15%.

There is a significant range of compositions where this material has properties better than single metal amorphous oxide films. The optimum composition was used in the thickness scan that follows.

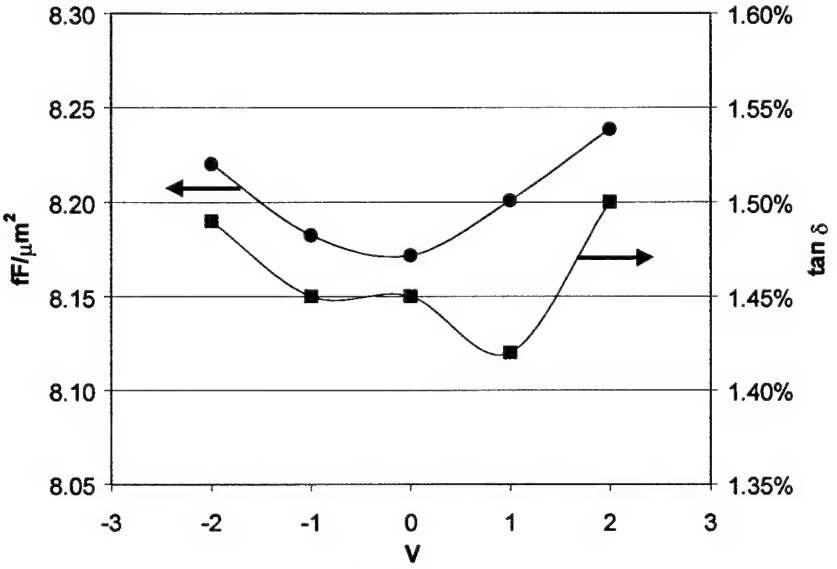



Figure 33. Capacitance density and loss as a function of bias voltage (room temperature measurement with 0.1V oscillation) for film 695.

**Amorphous high k low T dielectrics - Thickness scan**

This experiment was designed to examine the dielectric properties as a function of film thickness and deposition temperature at the composition that was identified as preferable in the broad composition scan of the previous experiment.

*Film Growth Details*

Films S44-57 were grown in a modified WJ reactor. The 150mm substrates had nominally 100nm Ir on 500nm thermal $SiO_2$ on Si <100>. Runs S56-57 were performed with test dies containing working transistors (see IC Process Integration, below) glued to the top of the substrate with silver paste. Run S56 was deposited at nominally 388 °C and run S57 was deposited at nominally 353°C, each with a 15 minute coat time and the solution composition appropriate for the temperature.

*Physical measurements*

The composition and thickness of all of the films was determined by XRF. The thickness values fwere normalized to RBS results with theoretical density, so they represent a lower limit to the physical thickness. The thickest films of each temperature, S44 and S53, were examined by XRD and no evidence of crystallinity in the films was evident as shown in Figure 34. The morphology was found to be independent of thickness as in Figure 35, but the surface roughness was observed to increase as a function of increasing deposition temperature, as shown in Figure 36.

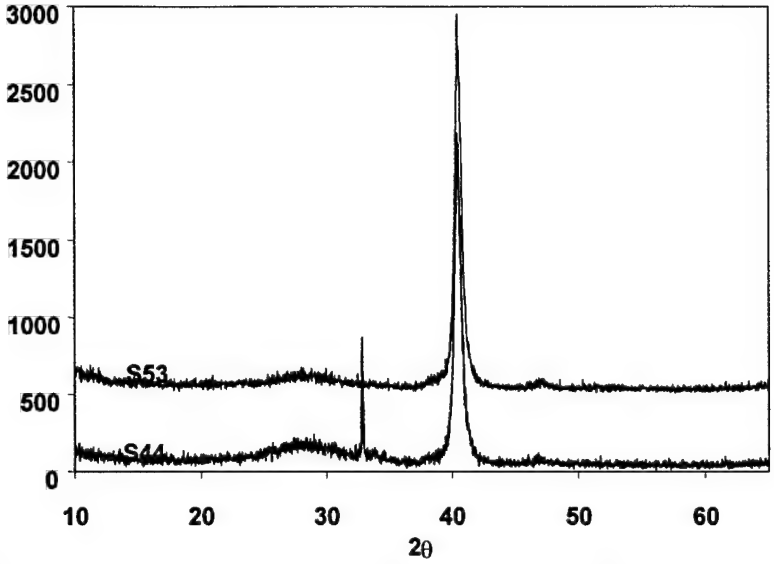



Figure 34. XRD spectra of films grown at 353°C (S44) and 388°C (S53) showing only an amporphous hump from the film.

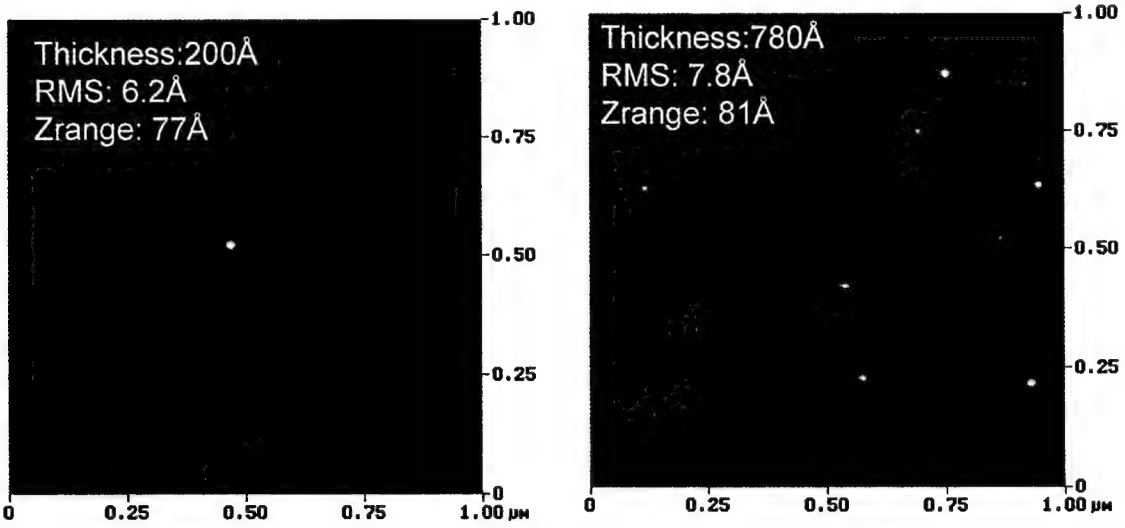



Figure 35. AFM scans over 1X1μm areas for films grown at 353°C. Note there may be a small increase in the film roughness with increasing thickness, but the roughness is similar to that of the bottom electrode.

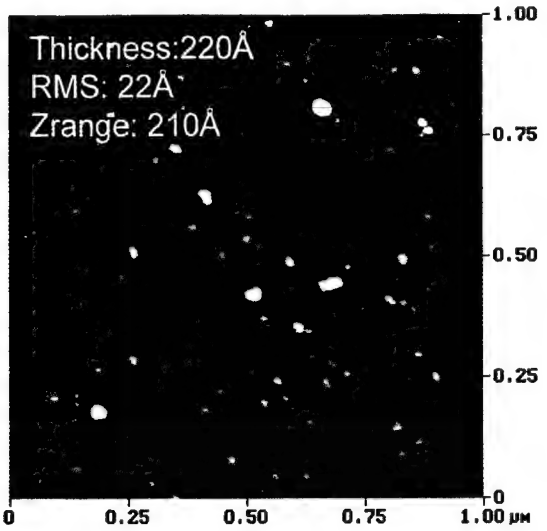



Figure 36. AFM scans over 1X1μm areas for a film grown at 388°C. Note a factor of 3-4 increase in the film roughness compared to films grown at 353°C.

*Electrical measurements*

Top electrodes were formed by e-beam evaporation of Pt through a shadow mask. The room temperature capacitance is plotted as a function of film thickness in Figure 37. The capacitance of the thinner films may be a little higher for the films grown at 390°C. The capacitance values measured here (in un-optimized films) of 10-25 fF/μm$^2$ were significantly greater than the values of 2-3 fF/μm$^2$ found in the best backend processes in current production.

The inverse capacitance is plotted versus thickness in Figure 38; the intercept is near zero, indicating a uniform dielectric constant, i.e., no "interfacial" capacitance as is often found with crystalline high dielectric materials.

The leakage behavior of these films was typified by two regimes separated by a "recoverable breakdown" as shown in Figure 39. The leakage in both regimes followed a generally log-linear behavior. The 520Å film in Figure 39 is a good thickness to demonstrate both regimes with the 20 V power supply of our leakage measurement system. Both the recoverable and non-recoverable breakdown voltages scaled linearly with film thickness for the films grown at 353°C, as shown in Figure 40. The recoverable breakdown occurred at a field of approximately 1.5MV/cm; the non-recoverable breakdown occurred at a field of approximately 3.0 MV/cm. The breakdown behavior of the films grown at 388°C was much less well defined with recoverable breakdown occurring at 0.4-0.9 MV/cm for a positive bias and at 1.7-2.2 MV/cm for a negative bias. Non-recoverable breakdown occurred at 1.0-1.3 MV/cm for a positive bias and 2.0-2.7 MV/cm for a negative bias. Considering the variation from capacitor to capacitor and the lower field breakdown for a positive bias, we believe that the roughness of the bottom electrode controls the breakdown. This is also consistent with the higher roughness seen in the AFM for the higher growth temperature films.

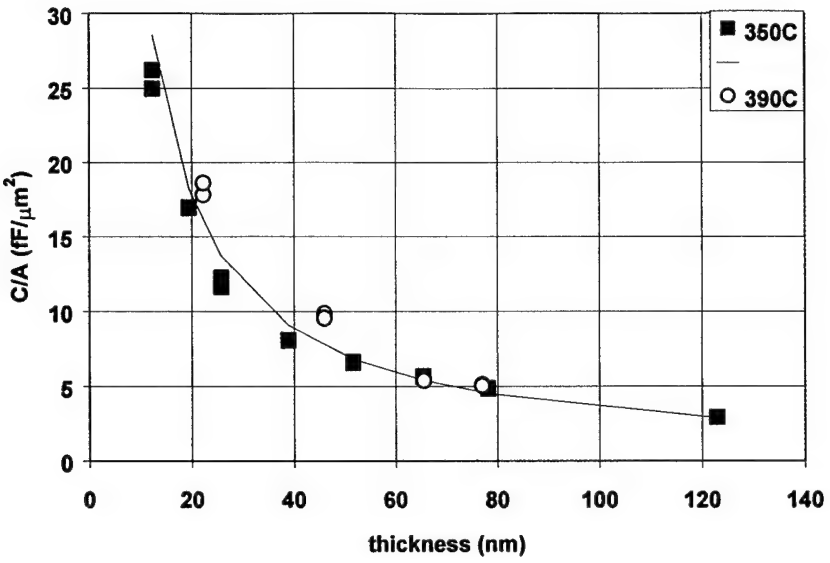



Figure 37. Capacitance as a function of film thickness for films grown at 353°C and 388°C.

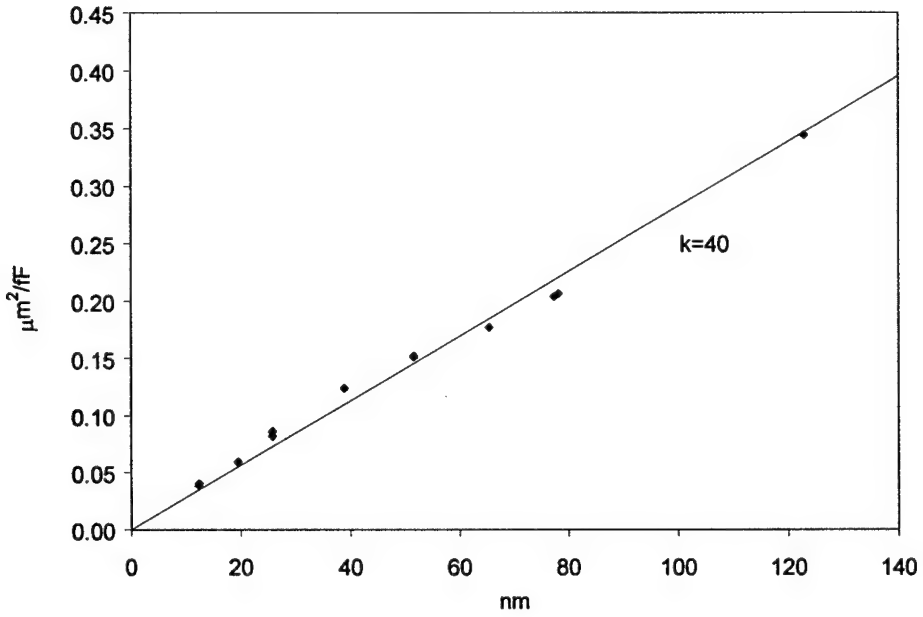



Figure 38. Inverse capacitance shows close to ideal behavior indicating little if any "interfacial" capacitance.

The leakage current as a function of film thickness is shown in Figure 41 at a constant field of about half the recoverable breakdown field. The leakage changes by less than a factor of 2, reinforcing our understanding of this material as nearly largely "bulk" (rather than interface) controlled.

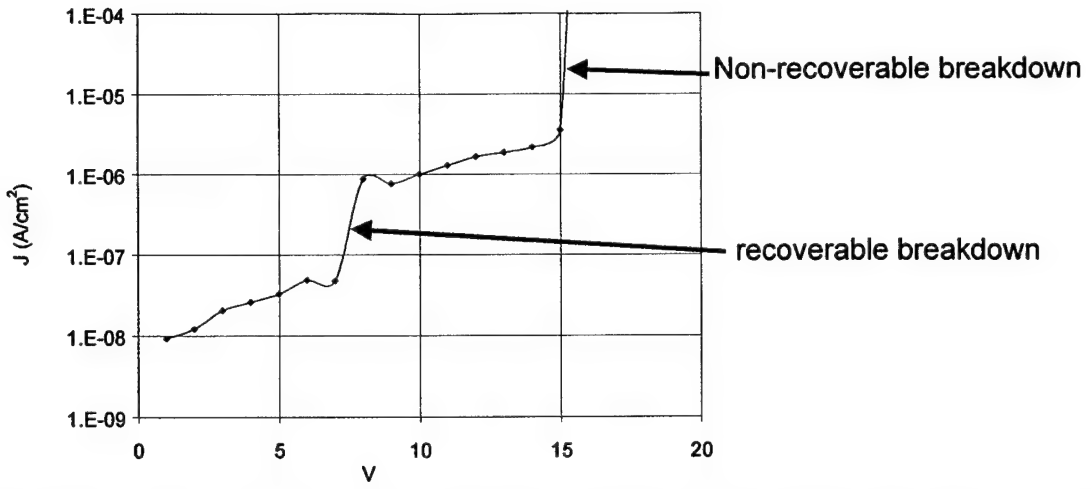



Figure 39. Leakage current as a function of voltage for sample S49 (520Å thick) showing two regimes of leakage separated by a "recoverable breakdown" and a "nonrecoverable breakdown" at higher voltages.

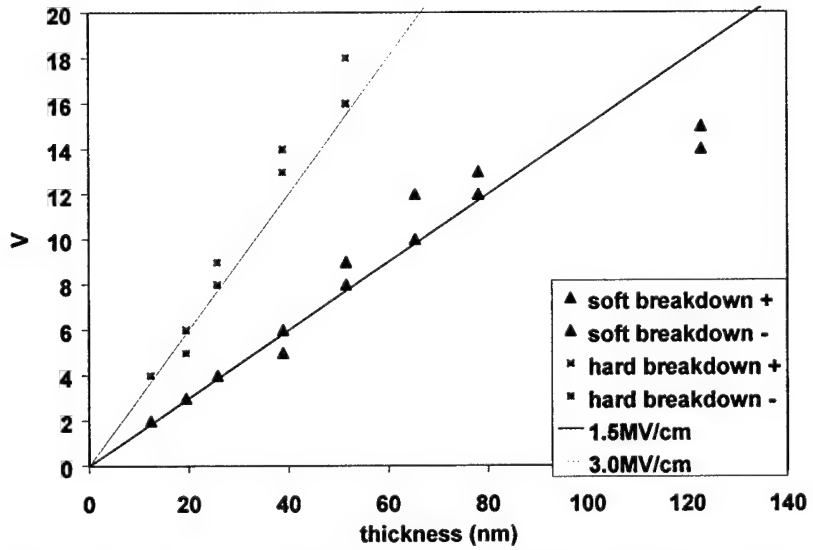



Figure 40. Breakdown voltages as a function of film thickness for films grown at 353°C. Soft breakdown occurs at about 1.5 MV/cm and hard breakdown at about 3 MV/cm.

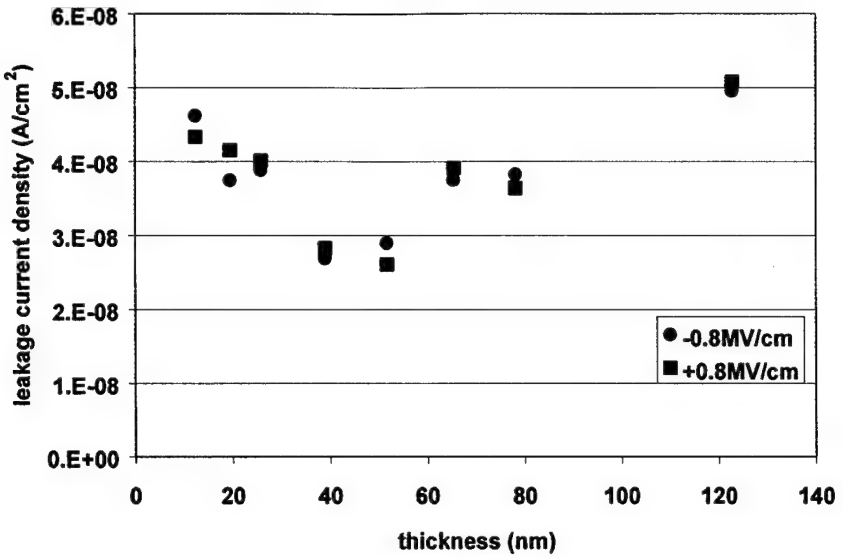



Figure 41. Leakage as a function of film thickness for a constant field of 0.8MV/cm.

## Cryogenic Measurements of Mixed Oxide Films

Samples from the thickness series, sample numbers 45-49 detailed in the phase I final report, were bonded and packaged in the same manner described for the BST samples above. Measurements were taken from top electrode to top electrode, placing two equivalent capacitors in series. The values reported here have been modified to reflect the average single capacitor behavior. Leakage and capacitance measurements were taken at ambient temperature and with the package immersed in liquid nitrogen. The leakage of each capacitor was measured until breakdown or the meter limit of 10V across each capacitor.

Figure 42 shows the change in capacitance density from ambient temperature to 77 K. The capacitance density decreased by about 10% upon cooling to 77 K. Figure 43 shows the decrease in loss at 100 kHz as the films are cooled to 77 K.

Leakage also decreases and breakdown increases upon cooling from ambient to 77 K. An example of the IV behavior is shown in Figure 44 for the 312 Å film. The breakdown field improves from 1.5 to over 3.0 MV/cm. This more than offsets the decrease in capacitance density as demonstrated in the approximate figure of merit shown in Figure 45.

*Conclusions*

These films show higher specific capacitance with low leakage than any other films known to the authors processed at less than 400°C. The capacitance scales well with film thickness indicating uniform field and dielectric constant through the thickness of the films. The breakdown behavior also scales well with thickness, confirming the uniform field through the dielectric. The figure of merit for these films improve at cryogenic temperatures. It appears that lower processing temperatures are advantageous for smooth film production although with proper

tuning of the bottom electrode structure, this may be easily overcome. The higher deposition temperature may have a slightly higher dielectric constant.

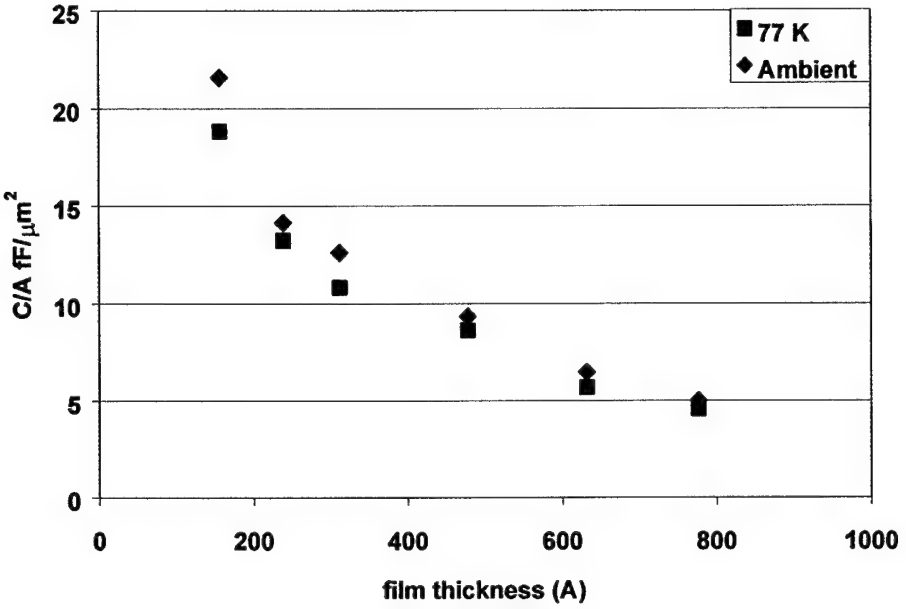



Figure 42. Capacitance density decreases by about 10 % as temperature drops from ambient to 77K in amorphous mixed oxide films.

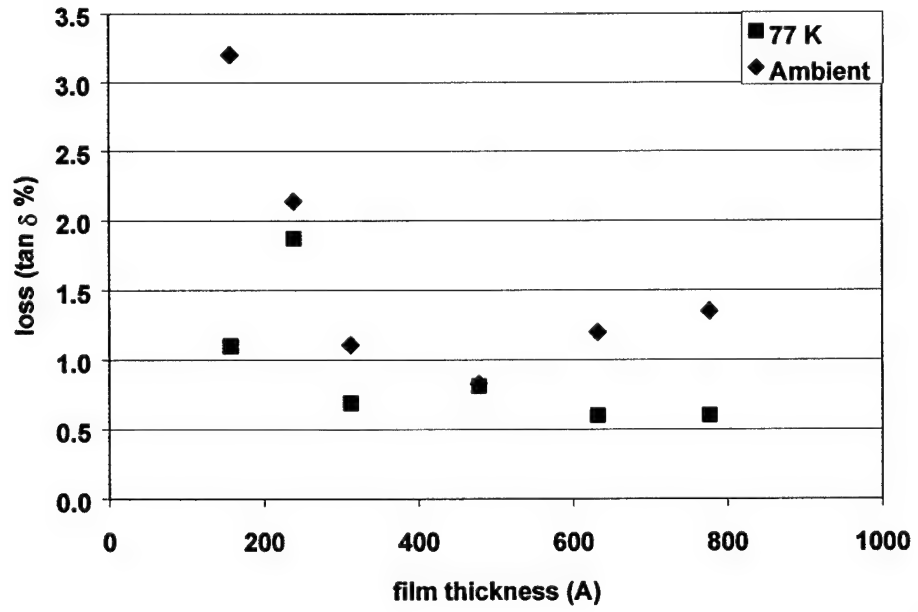



Figure 43. The loss of mixed oxide capacitors decreases significantly upon cooling from ambient to 77 K.

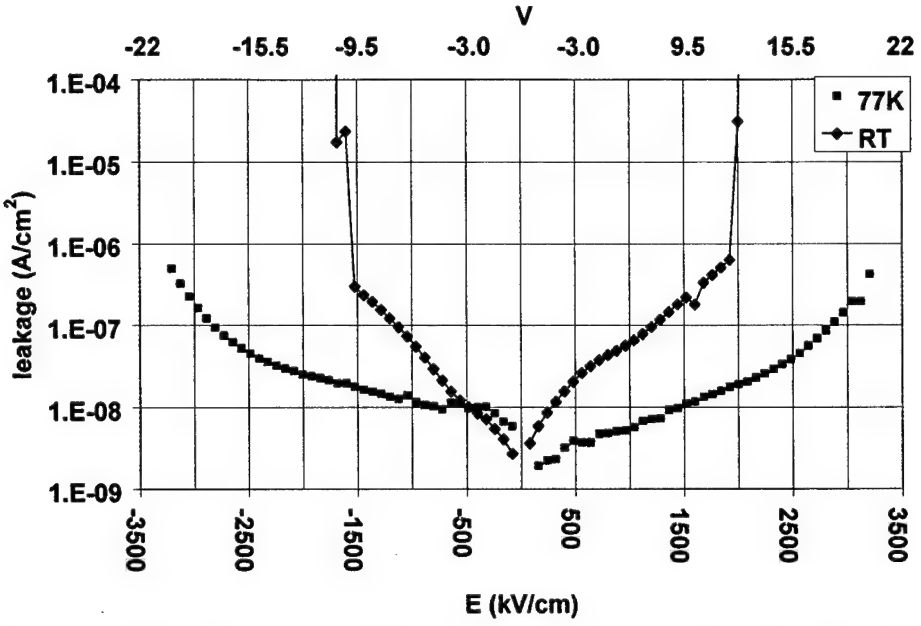



Figure 44. The leakage current is lower and the breakdown field increased by a factor of 2X as the temperature is lowered from ambient to 77 K.

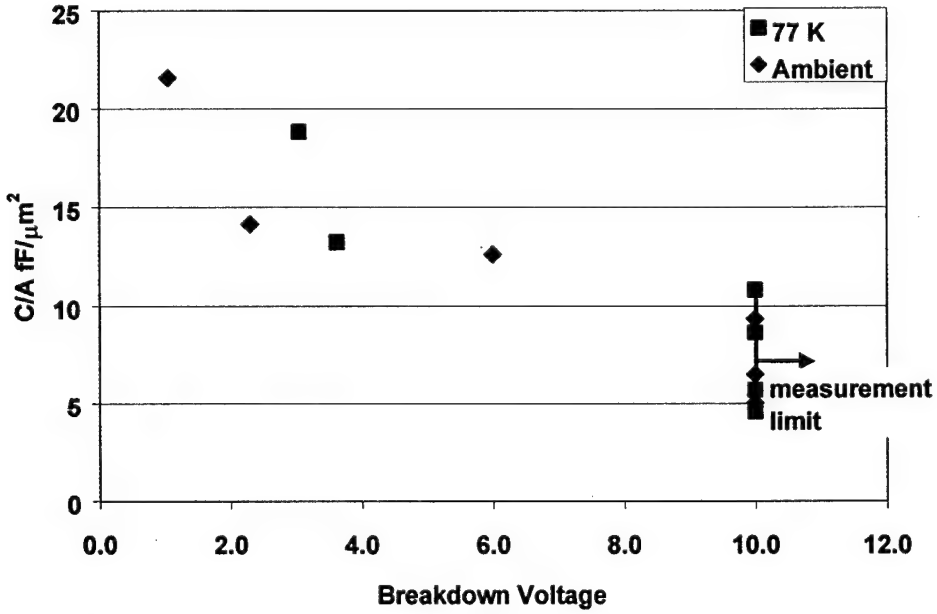



Figure 45. The capacitance available at any particular operating voltage is limited by the breakdown of the capacitor. The doubling of breakdown voltage more than compensates for the 10% loss in capacitance, giving mixed oxide films better performance at 77 K than at ambient temperature.

## Comparison of BST to mixed oxide films

In order to judge which of the two candidate materials provides the best solution, the cryogenic properties of BST and mixed oxide were plotted as a function of the maximum temperature during processing. BST grown at 450°C with various RTA temperatures is compared to the BST grown at 580°C and the mixed oxide grown at 350°C. Figure 46 shows that the dielectric constant of the BST grown at 580°C has a much higher dielectric constant than either of the other materials, but the mixed oxide has the best dielectric constant when the processing temperature is limited to below 500°C. Figure 47 shows that the mixed oxide capacitors showed the highest breakdown strength among these materials. Figure 48 shows the charge storage density of the different capacitor materials. The BST grown at 580°C clearly has the highest charge storage density, but among the lower processing temperature options, the mixed oxide has a higher storage density by a factor of 3 even though the processing temperature is 100°C lower than the amorphous BST.

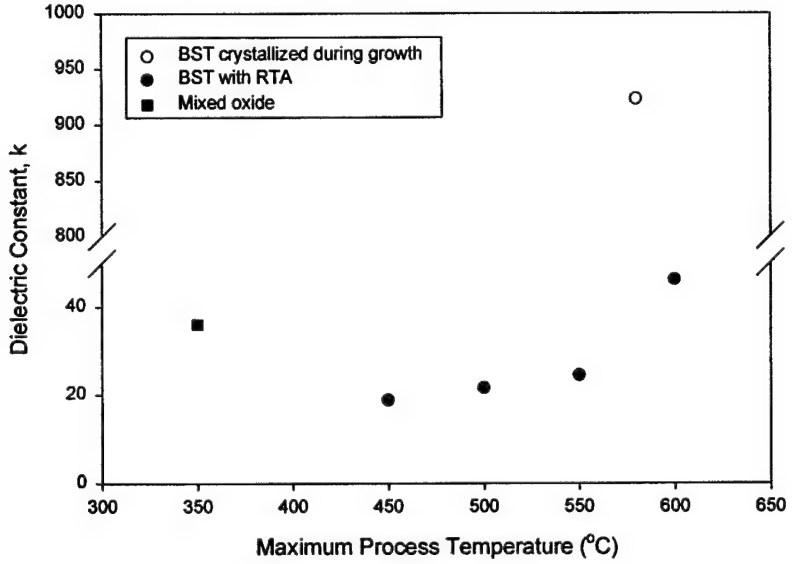



Figure 46. Dielectric constant at 77K as a function of the maximum processing temperature showing BST grown in the crystalline phase at 580°C has a much higher dielectric constant than the other materials. However, mixed oxide has a very high k for its growth temperature of 350°C.

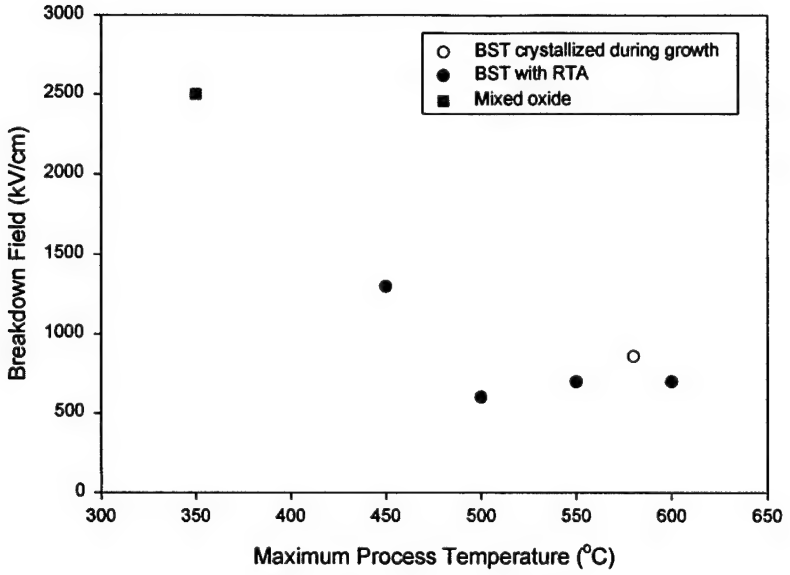



Figure 47. Breakdown field at 77K is shown as a function of the maximum processing temperature. Mixed oxide has the highest field strength and the lowest processing temperature.

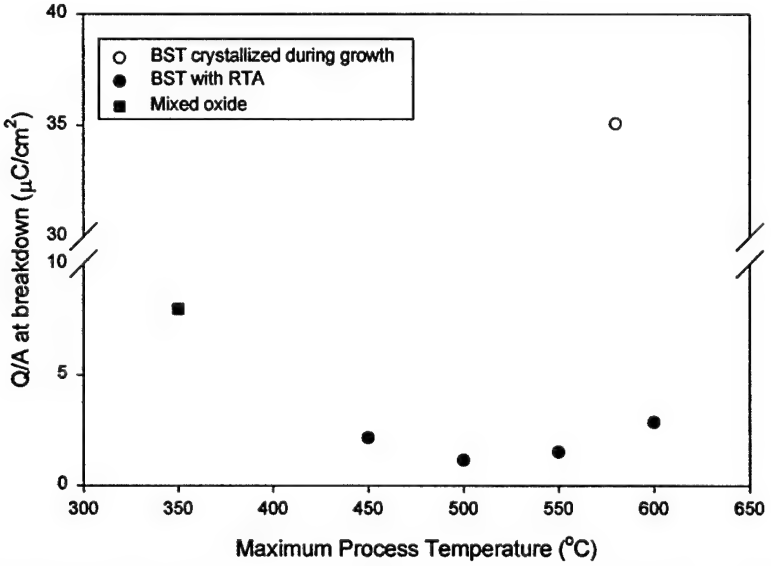



Figure 48. The charge per unit area at the breakdown field is shown as a function of the maximum processing temperature. The BST grown in the crystalline phase stores the most charge, however mixed oxide clearly outstrips the BST grown at lower temperatures, even after RTA to promote microcrystallization.

## *IC Process Integration*

With the success we had had in meeting the materials performance goals, the next step was to investigate the compatibility of the deposition process with the CMOS circuitry currently used for IRFPA. The first experiment was designed to determine if it is possible to integrate low temperature paraelectric storage capacitors into a foundry process. In this experiment, we subjected CMOS test chips to simulated conventional BST deposition conditions at different temperatures, see Table 13. The simulation consisted of a complete heating, deposition, and cooling cycle, with the exception that only solvent was used during the deposition, i.e. no metalorganics were introduced. The devices used for this process were produced using a 2μm foundry at Orbit Semiconductor. (The fab and process which produced these devices has since been sold to Supertex, which still provides it as a foundry service.)

Table 13. Simulated processing temperatures and times for the CMOS compatibility study

| SBRC Chip # | ATMI Deposition # | Date | Temperature (°C) | Time (s) |
|---|---|---|---|---|
| 14-3 | WJ2890 | 7/22/99 | 500 | 1200 |
| 14-6 | WJDummyA | 8/4/99 | 350 | 2000 |
| 14-7 | WJDummyB | 8/4/99 | 400 | 2000 |
| 14-8 | WJDummyC | 8/4/99 | 450 | 2000 |
| 14-9 | WJDummyD | 8/4/99 | 550 | 2000 |
| 14-10 | WJDummyE | 8/4/99 | 600 | 2000 |

The devices tested were n and p channel 100 μm /10 μm 1st poly gate MOSFETS which were available on existing process monitors. At all temperatures tested, a reduction in oxide trapped charge, Figure 49 and an increase in transconductance, Figure 50, was seen on the n-channel transistors. The reduction in oxide trapped charge can be seen as a shift to the left of the sub-threshold curves and the increase in transconductance can be seen as an increase in the drain current on the saturation curves. Both of these changes are small and in the direction of improved performance. These shifts can easily be accounted for during chip design, and are small enough that for most applications, no design changes will be necessary. At 600 °C, a small degradation can be seen in the p-channel sub-threshold characteristics. This degradation can be seen as a shift to the right indicating an increase in oxide trapped charge and a slight stretch-out of the sub-threshold swing which indicates interface state development, Figure 51. These changes are small and the devices are most likely useful in most circuits. If processing at this temperature is desired, it is recommended that further measurements be performed on these devices to determine impact on cryogenic performance and noise.

Test dies were also subjected to amorphous mixed oxide film deposition conditions, including exposure to precursor at both 350 °C, and 390 °C, and survived both temperatures with little to no measured change in device performance.

For future development, we need to consider much larger sample sizes in order to a statistical look at problems such as junction spiking. The best way to do this would be to run temperature cycles on completed wafers and look at total circuit performance. Testing a complete circuit would look at the performance of a statistically significant number of individual devices, and would more accurately indicate the effect of processing temperature on overall device performance.

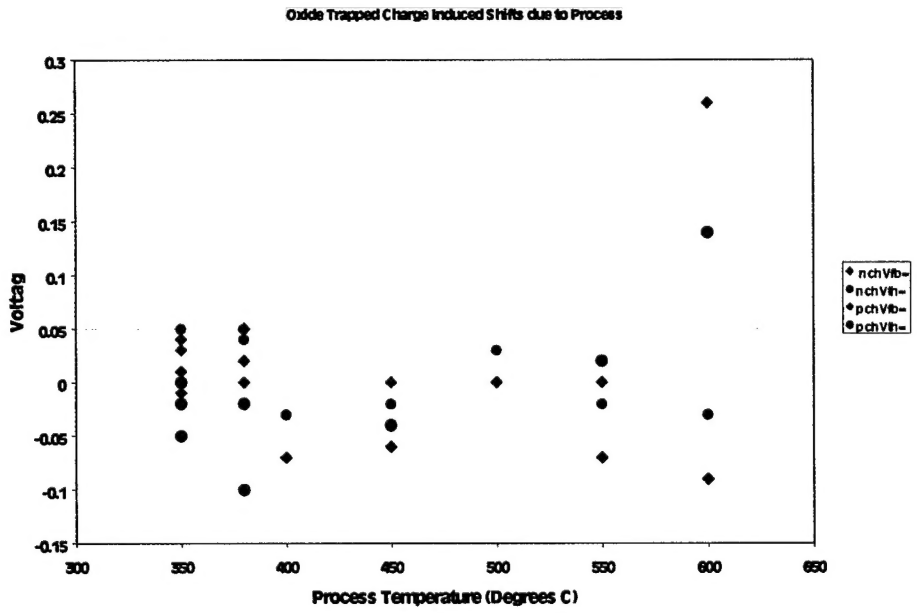



Figure 49. Voltage change due to oxide trapped charge as a function of simulated BST deposition on CMOS test chips

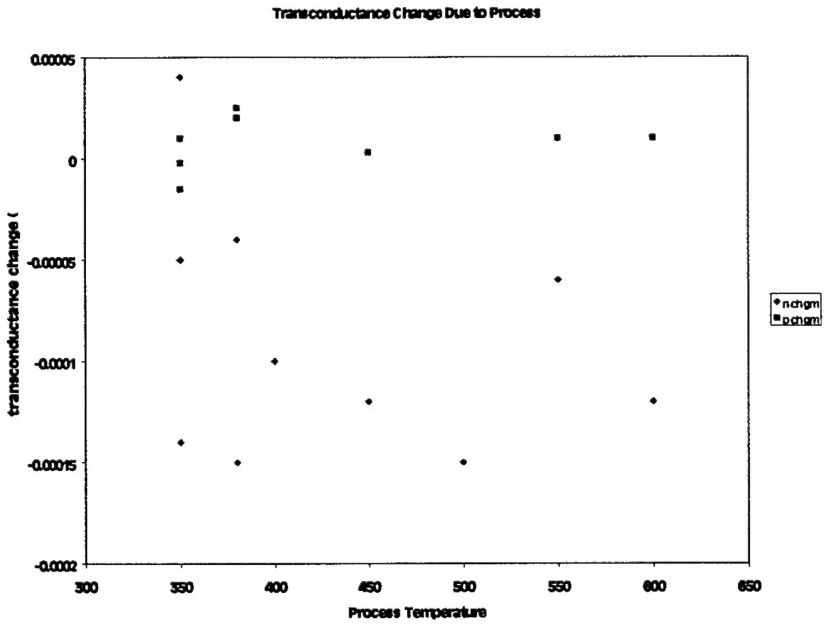



Figure 50. Transconductance change as function of simulated BST deposition on CMOS test chips

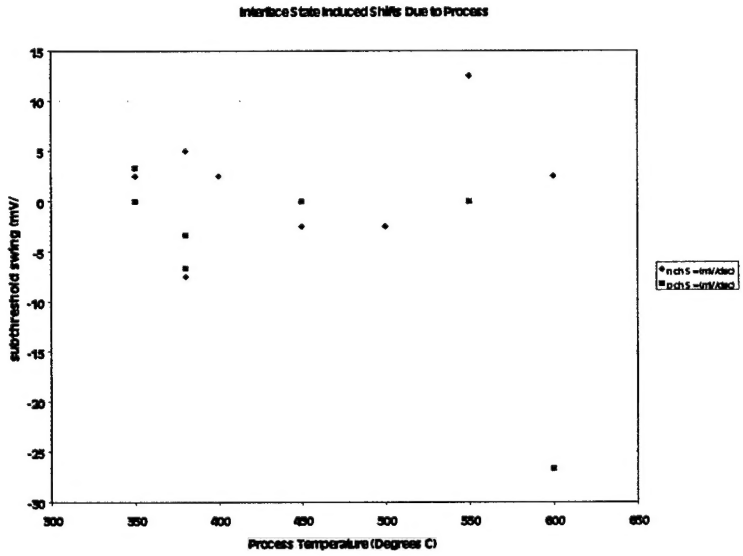



Figure 51. Subthreshold swing change as function of simulated BST deposition on CMOS test chips

## Summary and Conclusions

The purpose of this project was to enhance the performance of Infrared Focal Plane Array (IRFPA) detectors through the replacement of $SiO_2$ in the integrating capacitor of each array pixel by a material with a higher dielectric constant. In Phase II of this work, the following goals were achieved:

(1) The conventional MOCVD process for the cryogenic operation of BST thin films was optimized. The cryogenic storage capacity goal of 40 $fF/\mu m^2$ was exceeded, with an average storage capacity of 55 $fF/\mu m^2$, and a zero bias storage capacity of 90 $fF/\mu m^2$. Leakage current at 5V and 78 K was $2.3x10^{-7}$ $A/cm^2$ .

(2) A novel Digital MOCVD process for the fabrication of BST thin films was developed and patented. The deposition rate achieved using this technique exceeded the through-put requirement by factor of 2 in the best case. Further optimization of this process would be needed to yield films with electrical properties on par with those deposited the conventional process.

(3) RTA of BST films grown at 450 °C was examined as a low temperature alternative to conventional BST film growth in which films are crystallized *in-situ*. It was found that BST films of reasonable capacitance density can be grown in a low temperature MOCVD process. It was also found that RTAs can be used on these BST films on Pt to improve their dielectric constant and, to some extent, their capacitance densities (C/A) with modest improvements with a 600°C RTA. Finally, cryogenic properties of low temperature grown BST were measured for the first time, demonstrating that there is little change in dielectric constant but considerable improvement in leakage, giving increased C/A at these low operation temperatures, desirable for IR detector storage capacitors. In practice, it would be difficult to justify a low temperature MOCVD manufacturing process using this material due to low growth rates (~ 10 Å/minute) and difficulties with stoichiometry control in this growth regime.

(4) The use of low deposition temperature amorphous mixed oxide thin films for cryogenic applications was demonstrated. This was the first demonstration of a low temperature, high K process. Amorphous films deposited at 350 °C had storage densities as high as 25 $fF/\mu m^2$ at zero bias voltage, and represents a factor of 4 to 12 improvement over current $SiO_2$ technology. Based on the comparison in Figure 48, it can be seen that superior charge storage densities are available from mixed oxide in the lower temperature regime where integration into FPA read-outs would be performed. This, combined with superior growth rates (~ 40 Å/minute) and stoichiometry controllability in low temperature MOCVD, make mixed oxide the material of choice when growth temperatures are limited to 500 °C or less as in this application. It can offer significantly higher capacitance densities then current thin film capacitor technologies at cryogenic temperatures, showing great promise for Raytheon's FPA storage capacitor application.

(5) The MOCVD process compatibility with current CMOS chip technology was characterized. These experiments indicated that the temperatures required to achieve optimal storage density in a convention BST process (580 °C) may be acceptable for use with standard CMOS foundry processes based on transconductance and trapped charge measurements. Additional statistical studies of transistor properties are merited by these promising results.

In summary, we were able to meet or exceed many of the materials properties goals for this project using several viable alternatives that were compatible with CMOS circuitry. In addition, we developed a novel digital CVD process, and a new amorphous-oxide dielectric material system. These achievements lead us to conclude that is a realistic goal to incorporate these materials in a working IRFPA, and that significant device performance improvements would be realized by doing so.